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# MULTI-TRAK
# MODEL 615

# SYNTHESIZER/SEQUENCER

# TECHNICAL MANUAL

by Chet Wood

and Stanley Jungleib

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MULTI-TRAK
MODEL 615

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## Table of Contents


| | TOPIC | PAGE |
|---|---|---|
| **SECTION 1** | **GENERAL DESCRIPTION** | |
| | Overview | 1 |
| | Digital circuitry | 1 |
| | Inputs | 2 |
| | Generating control signals | 2 |
| | Outputs | 2 |
| | Tuning | 3 |
| | Synthesizer circuitry | 3 |
| | Audio circuitry | 4 |
| | Figure 1: Abstract schematic | 5 |
| **SECTION 2** | **SYSTEM/CHASSIS** | |
| | Abnormal power-on indications | 7 |
| | Resetting the sequencer | 7 |
| | Initializing the pitch wheel | 7 |
| | Updates | 7 |
| | Mechanical disassembly/reassembly | 8 |
| | Board extender | 9 |
| | Parts list/functional description | 10 |
| **SECTION 3** | **PCB 1** | |
| | Schematics for PCBs 1 and 2 | |
| | Sheet A | 15 |
| | Sheet B | 16 |
| | Sheet C | 17 |
| | Designator map, PCB 1 | 18 |
| | Designator map, PCB 2 | 19 |
| | Parts list/functional description (PCB 1) | |
| | Integrated circuits | 20 |
| | Passive components | 21 |
| | Non-designated components | 21 |
| **SECTION 4** | **PCB 2** | |
| | Keyboard scanner reset problem | 23 |
| | Parts list/functional description | |
| | Integrated circuits | 23 |
| | Passive components | 34 |
| | Non-designated components | 35 |

**SECTION 5 PCB 3**


Schematics for PCB 3
- Sheet D 39
- Sheet E 40

Designator map, PCB 3 41

DAC trim 42
- Figure 2: Trimmer and test point locations 42

Audio out field update 43
- Figure 3: Silkscreen 44
- Figure 4: Component side traces 45
- Figure 5: Solder side traces 46

Parts list/functional description
- Integrated circuits 47
  - Figure 6: 3394 block diagram 51
- Passive components 59
- Non-designated component 63

## SECTION 1 GENERAL DESCRIPTION

### Overview

The 615 ("MULTI-TRAK") from Sequential is a polyphonic voltage-controlled hybrid (digital plus analog) synthesizer. Six 'voice-on-a-chip' voices are controlled by a Z-80A microprocessor system. Included are a velocity-sensitive keyboard scanned by a 6801 microcomputer, a switch panel with LED displays, multi-timbral sequencer, MIDI computer interface, and multiple audio outputs.

Note: For operation information, see the Operation Manual (CM615), Instruction Card (CN615-1), Controls and Indicators Card (CN615-2), and MIDIGUIDE (MG615).

The instrument has been produced in two basic versions. The first, rev B, has several modifications to the PC boards to improve performance. Early rev B's may not have all the mods installed, and should be updated. Rev C, in addition to incorporating these mods onto the boards, has a redesigned PCB 2, which uses different non-volatile memory chips. Note: Rev C schematics and designator map are contained in a separate document.

To determine which rev of the instrument you are working on, look at the circuit boards. Each board has a rev letter clearly marked on the component side silkscreen. Rev A boards are electrically the same as rev B, so any mix of rev A and B boards can be used in a rev B instrument.

While reading the following general circuit description, it may be helpful to refer to the abstract schematic, page 5.

### Digital circuitry

The Z-80A microprocessor (CPU) is the heart of the 615. It accepts control inputs, generates and sums control signals, sends them to the analog synthesizer circuitry, and checks the oscillator tuning. The interface between the CPU and the synthesizer is primarily via the DAC and demultiplexers. Also associated with the CPU are four signal generators for each voice: a low frequency oscillator (LFO) and three envelope generators. Although functionally part of the voices, they are generated in software by the CPU.

### Inputs

The CPU is itself controlled by the keyboard, front panel switches, MIDI interface, and sequencer. The keyboard scanner constantly checks the keyboard, and interrupts the CPU when a key event occurs. The switches and pots are periodically checked by polling to see if any have changed. MIDI inputs interrupt the CPU, forcing it to respond immediately. And the sequencer, through physically not separate from the CPU, advances at precise intervals and initiates events as it has been programmed.

### Generating control signals

When an input event happens, the CPU changes the signals it is sending to the voices or using to control itself. For instance, when a key is pressed, a voice must be assigned to play it, the frequency control voltage must be calculated and corrected for tuning errors, the envelopes must be initiated, etc.

Between events, also, the CPU is busy. Every seven milliseconds it must advance each envelope, LFO, and glide, and add the latest value into other control signals. Sequencer timing is handled by the CPU with minimum overhead by means of an outboard counter, which is programmed to interrupt the CPU at the next sequencer clock. When interrupted, the CPU synchronizes the internal sequencer clock.

### Outputs

All the control signals the CPU generates must be applied to various outputs: the voices, the LEDs, the sequencer, and MIDI.

The voices are controlled by 48 control voltages, which are generated by the DAC, demultiplexers, and sample/holds. Every voice has eight control voltage inputs, and they must all be updated every seven milliseconds. The CPU sends data representing required voltages to the DAC one at a time, and after allowing the DAC to settle, opens the demultiplexer for that voltage and voice. After charging the sample/hold capacitor to the DAC voltage, the demultiplexer opens the path to that capacitor and the next number is sent to the DAC, the next cap selected, and so forth, until all 48 sample/holds have been updated. This takes two to three milliseconds.

In contrast, the LEDs are quite simple to control. Panel LEDs are separated into several multiplexed banks, each bank being turned on for a few milliseconds while the others are off. This creates the illusion of a steady display.

Finally, most input events are relayed to the outside world through MIDI, and, in record mode, are recorded in the sequencer memory.

## Tuning

Due to temperature drift and component aging, the analog oscillators in the 615 must be corrected to remain in tune. The CPU measures the frequency of each oscillator and determines the correction required for it to play in tune. When power is first applied, the voices use the tuning corrections established the last time power was on. Then, after every 30 seconds of "standby" time (power on but all voices' envelopes fully decayed), the 615 tunes one voice.

In preparation for tuning, the audio output is shut off by the audio enable switch, a sawtooth wave selected, the filter and amplifier opened for the voice to be tuned, and other voices disabled. The voice is tuned at seven C's over the range of the oscillator. First, the voltage that was last known to produce that C is applied through the DAC. If the measured frequency is correct, the next C is tuned. If not correct, the voltage is incremented or decremented one step at a time, until it is in tune. This result is stored, so when this C is later played, the voltage required to produce it is known. If a note other than a C is played, its control voltage is found by interpolating within the octave. The entire tuning process for a voice takes about ½ second, and is fully interruptible, should a keystroke or MIDI input occur during the process.

If a voice is so far out of tune that a few increments or decrements cannot bring it in, successive approximation is used. To begin, the most significant bit (MSB) of the DAC is set high and all others zeroed. The resulting oscillator frequency is then measured by U220 SCI Combo Chip and the result compared to the desired frequency. If it is higher than desired, the MSB is reset, otherwise it is set. Then, the next most significant bit is set, a trial made, and so on until the exact voltage is determined.

## Synthesizer circuitry

The analog synthesizer portion of the 615 consists of the six voice chips (described under U315 in Section 3), a noise generator for all six voices, and a comparator for feeding back audio signals to the tune counters located on U220 combo chip.

Since all controls for each voice are separate, true multi-timbral synthesis is possible with the 615.

## Audio circuitry

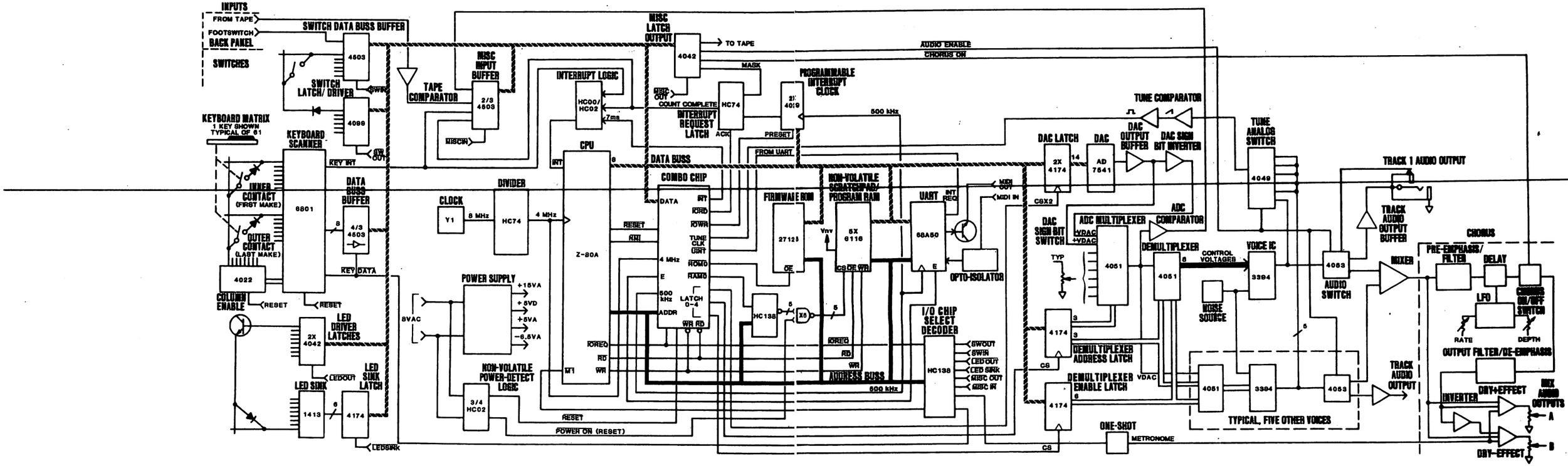
Audio circuitry falls under two main categories: audio switches and buffers, and the chorus section.

The audio switches and buffers provide for the audio to be muted during the tune routine, and for the voices to be mixed together or brought out separately. If an individual voice output is used, its signal is cut off from the mixed output.

The chorus circuit comprises the following stages:

- Pre-emphasis
- Anti-aliasing filter
- Delay line
- Smoothing filter
- De-emphasis
- Phase inversion
- Output mixing, for 'dry + effect' and 'dry - effect' signals

The delay line is driven by a high-frequency sampling clock which is controlled by a sine-wave LFO, whose depth and rate are adjustable. If the chorus is switched off, **Mix A** and **B** outputs are identical.


INPUTS
FROM TAPE
FOOTSWITCH
BACK PANEL
SWITCHES
SWITCH DATA BUSS BUFFER
4503
SWITCH LATCH/ DRIVER
4099
KEYBOARD MATRIX
1 KEY SHOWN
TYPICAL OF 61
KEYBOARD SCANNER
6801
INNER CONTACT (FIRST MAKE)
OUTER CONTACT (LAST MAKE)
4022
COLUMN ENABLE
RESET
DATA BUSS BUFFER
4/3 4503
KEY INT
KEY DATA
LED DRIVER LATCHES
2X 4042
LED SINK
1413
LED SINK LATCH
4174
LEDSINK
TAPE COMPARATOR
MISC INPUT BUFFER
2/3 4503
MISCIN
INTERRUPT LOGIC
HC00/ HC02
CPU
Z-80A
DIVIDER
HC74
CLOCK
Y1
8 MHz
4 MHz
POWER SUPPLY
8VAC
+15VA
+5VD
+5VA
-6.5VA
NON-VOLATILE POWER-DETECT LOGIC
3/4 HC02
POWER ON (RESET)
MISC LATCH OUTPUT
4042
TO TAPE
AUDIO ENABLE
CHORUS ON
MASK
COUNT COMPLETE
INTERRUPT REQUEST LATCH
HC74
ACK
PROGRAMMABLE INTERRUPT CLOCK
2X 4019
PRESET
FROM UART
500 kHz
DATA BUSS
COMBO CHIP
DATA
INT
IORD
IOWR
TUNE CLK
UINT
ROMD
RAMD
LATCH 0-4
ADDR
WR RD
FIRMWARE ROM
27128
NON-VOLATILE SCRATCHPAD/ PROGRAM RAM
5X 6116
UART
68A50
OPTO-ISOLATOR
MIDI OUT
MIDI IN
HC138
X6
I/O CHIP SELECT DECODER
HC138
SWOUT
SWIN
LED OUT
LED SINK
MISC OUT
MISC IN
ADDRESS BUSS
DAC LATCH
2X 4174
DAC
AD 7541
DAC OUTPUT BUFFER
DAC SIGN BIT INVERTER
TUNE COMPARATOR
TUNE ANALOG SWITCH
4049
TRACK 1 AUDIO OUTPUT
TRACK AUDIO OUTPUT BUFFER
DAC SIGN BIT SWITCH
ADC MULTIPLEXER
ADC COMPARATOR
4051
DEMULTIPLEXER
CONTROL VOLTAGES
VOICE IC
3394
NOISE SOURCE
4053
AUDIO SWITCH
MIXER
CHORUS
PRE-EMPHASIS/ FILTER
DELAY
LFO
CHORUS ON/OFF SWITCH
RATE
DEPTH
OUTPUT FILTER/DE-EMPHASIS
DEMULTIPLEXER ADDRESS LATCH
DEMULTIPLEXER ENABLE LATCH
4174
CS
VDAC
TYPICAL, FIVE OTHER VOICES
TRACK AUDIO OUTPUT
INVERTER
DRY+EFFECT
MIX AUDIO OUTPUTS
A
B
DRY-EFFECT
ONE-SHOT
METRONOME

### Abnormal 'power-on' indications

When power is first switched on, the **Value/Program** display should read '00' and one of the **Seq** LEDs should light. **Chorus On/Off** may also light. If instead, the instrument goes through a tune routine, indicated by a slow count from 1 to 6 in the **Value/Program** display, there may be a problem with non-volatile memory. Save programs, sequences and stacks on tape (see the operation manual), then troubleshoot the non-volatile power supply, memory chips and associated circuitry.

### Resetting the sequencer

If the sequencer does not operate, and you are not making an operational error, first save the sequences to tape, then reset the sequencer. Switch on **SEQUENCER Record**, then hold **Seq** and press **Program Record.**

---

CAUTION: This procedure destroys all sequences in memory.

### Initializing the pitch wheel

If recorded sequences play back in a different tuning than they were recorded in, or voices go out of tune with each other when the pitch wheel is moved, the pitch wheel may need initializing. Hold **Program Record** and press **3**, then move the wheel and return it to center.

### Updates

Three conditions exist in early production models which should be repaired under warranty if a customer complains:

1. Hum or noise in the audio output. See p. 43 for update procedure. (S/N less than 684.)

2. Occasionally, when power is first turned on, the keyboard does not work until a certain key is hit or power is turned off and back on. See page 20. (S/N less than approximately 100.)

3. The pins of P202 can short to traces near J302, causing various symptoms. To correct this problem, add a 4-40 external star lockwasher between each of the two 4-40 standoffs and PCB 3. (Alternatively, with a pair of diagonal cutters, carefully trim a small amount from the length of each of the pins of P202.)

**Mechanical disassembly**

1. Turn off power and remove power cord from the rear panel connector.

2. Of the five screws on each side panel, remove the top two and loosen the remaining three.

3. Remove four screws on the rear, holding the top panel to the bottom panel.

4. Remove the top panel from the chassis. There should be enough keyboard cable so that the panel may be propped up in a working position without disconnecting the cable. Be careful not to scratch the panel. Place it on a protective pad.

5. Power may be reapplied and the unit tested in this position.

6. To gain access to the computer board (PCB 2), first unplug the power supply cable that runs from PCB 1 to PCB 3, then remove PCB 3 by removing the 5 6-32 screws and 2 4-40 screws holding it to PCB 2. Finally, gently pull PCB 3 out, disengaging the connectors holding it to PCB 2.

7. Boards 1 and 2 must be removed together. First, pull the knobs off from the top and remove the pitch/mod wheel cable. Then remove the 5 6-32 screws holding PCB 1 and the 4 6-32 screws holding PCB 2. With a ¼" nut driver, remove the 5 M-F threaded standoffs holding PCB 2.

**Mechanical reassembly**

1. Reverse order of disassembly.

2. When installing PCB 2 to the top panel, be careful to put the 2 4-40 M-F threaded standoffs into the smaller holes, and the 3 6-32 standoffs into the holes that match up with the mounting holes in PCB 3.

CAUTION: Do not over-tighten the standoffs!

3. When installing PCB 3, line up the connectors carefully before plugging it in to PCB 2. Be sure to install lockwashers between all standoffs and PCB 3. Install the 2 4-40 screws into the smaller holes.

4. Test unit to make sure the keyboard and wheels have been plugged in. Test the **Master Volume** and **Master Tune** controls. If they do not work, the PCB 3 to PCB 2 connectors may not have been lined up.

5. Tighten all screws.

## Board extender

Ordinarily, troubleshooting of PCB 1 or PCB 2 can be done with PCB 3 removed. However, in a few cases, PCB 3 must be installed and operating while probing test points on PCB 2. For this purpose, a board extender kit, SCI part number PC-0615-BS, is available. The kit consists of a PCB that can be used with ordinary double-row header cables. The cables themselves are not supplied by Sequential.

| DESIGNATOR | SCI PART# | DESCRIPTION |
|---|---|---|

## PARTS LIST/FUNCTIONAL DESCRIPTION

### PASSIVE COMPONENTS

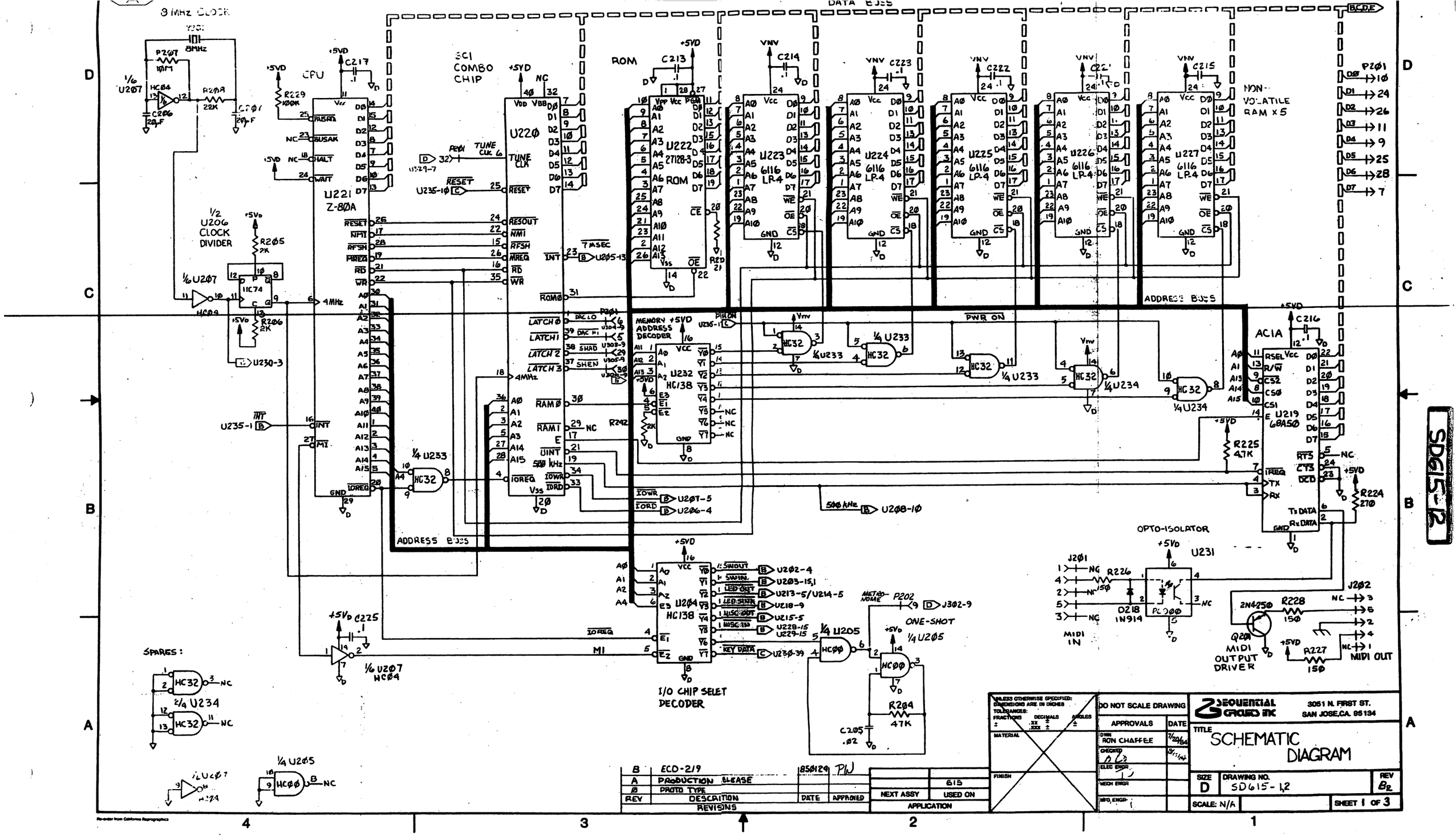
| | | |
|---|---|---|
| PS1 | E-170 | 15VAC 1-¼A CT WALL MOUNT 110V |
| | E-175 | 15VAC 1-¼A CT WALL MOUNT-220V |
| R1,R2 | R-207 | 100K LINEAR POTENTIOMETER<br>Function: Pitch, mod wheels |
| W1 | S-090 | 5 OCTAVE WEIGHTED VELOCITY, PANASONIC SK7020<br>Function: Keyboard |

### NON-DESIGNATED PARTS

| | |
|---|---|
| 870 | 615 FACTORY PROGRAM TAPE |
| E-173 | 9" RIBBON CABLE W/FEMALE .1" RECEPTACLE |
| M-016 | LARGE RUBBER FEET |
| M-071 | 6-32 X 1/4" PAN HD PHIL MS |
| M-199 | 4-40 X 1/4" BLACK PAN HD PHIL |
| M-357 | BLACK KNOB .250 X .156 |
| M-383 | #4 STAR WASHER EXT TOOTH |
| M-420 | #8 X 5/8" BLACK SHEETMETAL PAN HD PHIL |
| M-438 | RED ACETATE WINDOW 1.25"X 1.75"X 10 ml |
| M-475 | #8x1/4 BLACK PAN HEAD SMS |
| M-481 | 10-32 x 3/8 BLK PAN HD PHIL |
| M-498 | 6-32 MALE/FEMALE 5/8" HEX STANDOFF |
| M-505 | 4-40 X 5/8" THREADED STANDOFF |
| M-506 | #8 X 3/8" BLACK SHEETMETAL PAN HD PHIL |
| M-507 | M5-5 (METRIC) CHEEZE HEAD SCREW |
| MW0615-1 | 615 TOP PANEL |
| MW0615-2 | 0615 BOTTOM PANEL |
| PC0615-BS | PCB 3 to PCB 2 extender kit (less cables)<br>(For service use only) |
| PW0620-1 | PLASTIC END CAP LEFT |
| PW0620-2 | PLASTIC END CAP RIGHT |
| Z-339 | HALF CUT MOD WHEEL SUBASSEMBLY |

| DESIGNATOR | SCI PART# | DESCRIPTION |
|---|---|---|
| | J-056 | 5 PIN HOUSING |
| | M-070 | 6-32 X 1/2" SET SCREW |
| | M-090 | 6-32 HEX NUT |
| | M-192 | #8 BLACK FLAT WASHER |
| | M-384 | 1/8" X 1/8" ALUM RIVET |
| | M-397 | 6-32 X 7/8" PAN HD PHIL |
| | M-485 | PITCH WHEEL SNAP BUTTON |
| | M-497 | #6 INTERNAL TOOTH LOCK WASHER |
| | MW0000-2 | MOD WHEEL BRACKET 1/HT |
| | PW0000-1 | MOLDED HALF CUT MOD WHEEL |

Function: Pitch and mod wheels. Has set screw.




| REV | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| B | ECO-219 | 850124 | PW |
| A | PRODUCTION RELEASE | | |
| Ø | PROTO TYPE | | |

REVISIONS

| NEXT ASSY | USED ON |
|---|---|
| | 615 |

APPLICATION

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES
TOLERANCES: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH

DO NOT SCALE DRAWING

| APPROVALS | DATE |
|---|---|
| DWN RON CHAFFEE | 7/20/84 |
| CHECKED | 8/17/84 |
| ELEC ENGR | |
| MECH ENGR | |
| MFG ENGR | |

SEQUENTIAL CIRCUITS INC
3051 N. FIRST ST.
SAN JOSE, CA. 95134

TITLE SCHEMATIC DIAGRAM

SIZE D | DRAWING NO. SD615-1,2 | REV B2

SCALE: N/A | SHEET 1 OF 3

SD615-12

Re-order from California Reprographics

LED DRIVER LATCHES

LED DRIVERS

NC pins: 1,7,8,14

(PROGRAM)

(PROG)

(TRACK)

ADDRESS BUSS

SWITCH DRIVER

FOOT SWITCH

SWITCH DATA BUS BUFFER

LED SINK LATCH

LED SINK

MISC. OUTPUT LATCH

COUNTER INTERRUPT MASK

TO TAPE

1.9 KHz CLOCK DIVIDER

PROGRAMMABLE INTERRUPT CLOCK

INTERRUPT REQUEST LATCH

TAPE COMPARATOR

FROM TAPE

ADC COMP

MISC. INPUT BUFFER

COUNT COMPLETE

KEY INT

| | |
|---|---|
| NEXT ASSY | USED ON |
| APPLICATION | 615 |

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: FRACTIONS ±, DECIMALS .XX ±, .XXX ±, ANGLES ±. MATERIAL. FINISH.

DO NOT SCALE DRAWING

| APPROVALS | DATE |
|---|---|
| DRWN | 8/13/84 |
| CHECKED | 8/17/84 |
| ELEC ENGR | |
| MECH ENGR | |
| MFG | |

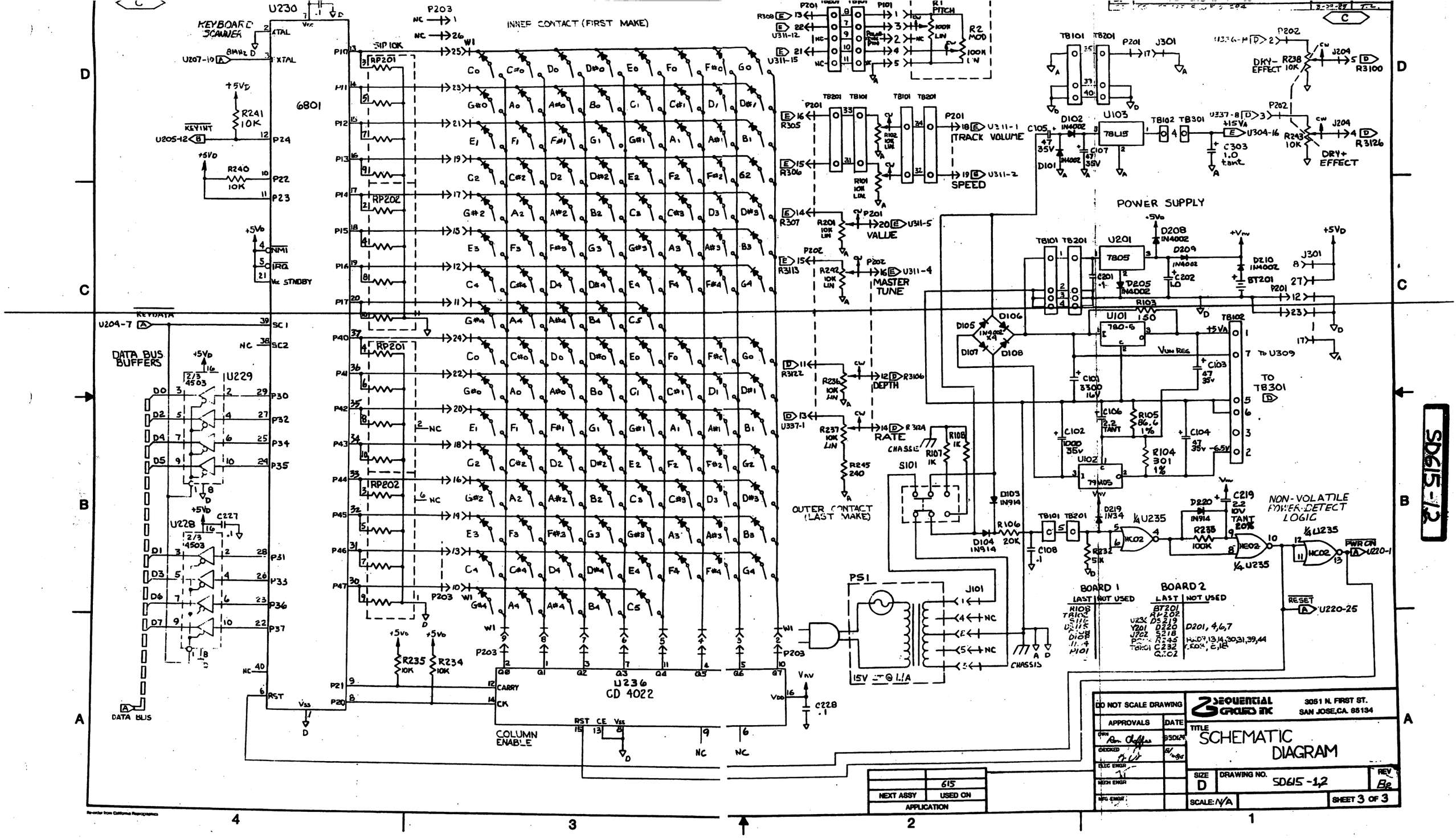
SEQUENTIAL CIRCUITS INC. 3051 N. FIRST ST. SAN JOSE, CA. 95134

TITLE: SCHEMATIC DIAGRAM

SIZE D | DRAWING NO. SD615-1,2 | REV B2

SCALE: N/A | SHEET 2 OF 3

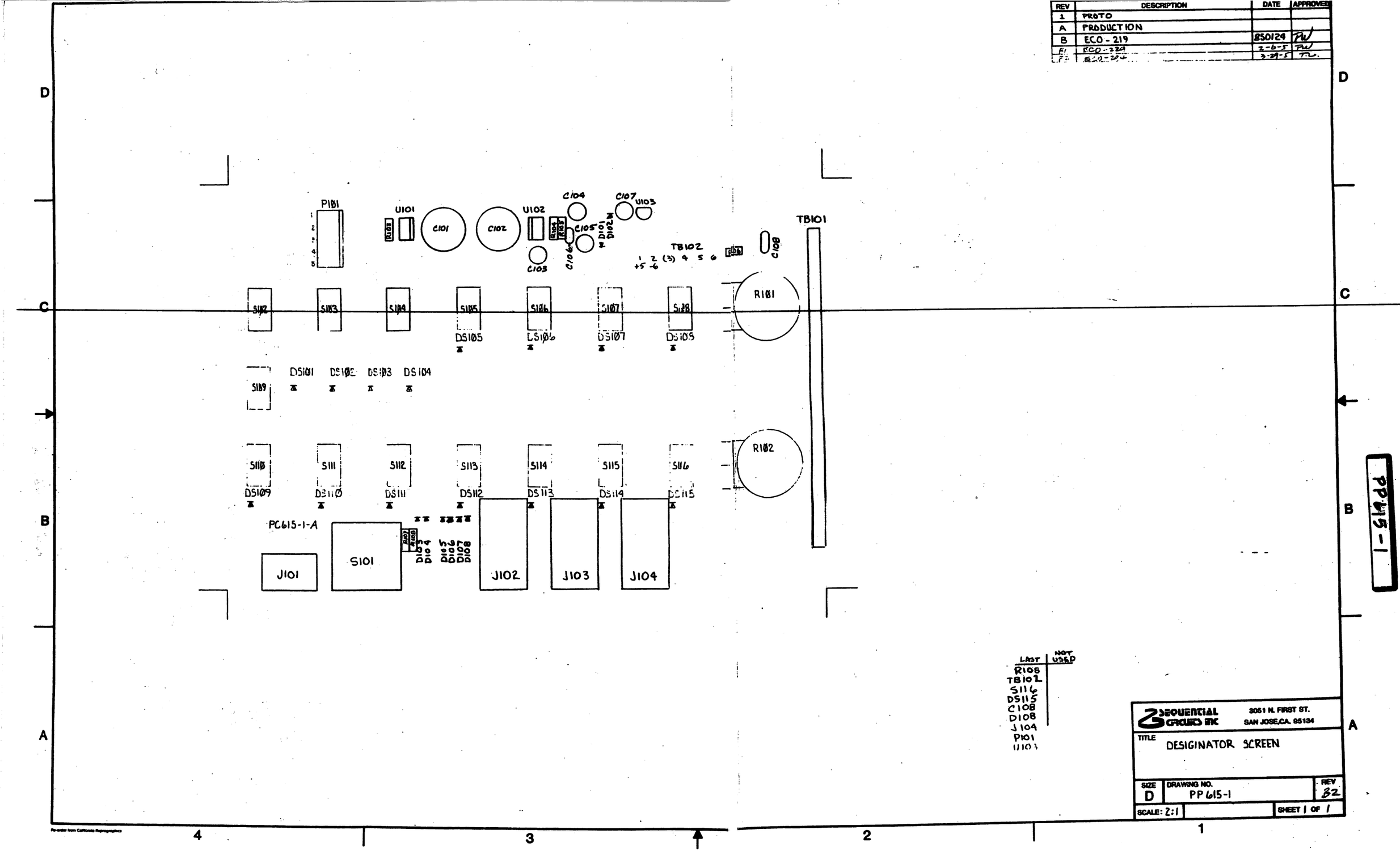
SD615-1,2



KEYBOARD SCANNER
6801
INNER CONTACT (FIRST MAKE)
OUTER CONTACT (LAST MAKE)
DATA BUS BUFFERS
DATA BUS
U229
U228
U230
U236
CD 4022
COLUMN ENABLE
TRACK VOLUME
SPEED
VALUE
MASTER TUNE
DEPTH
RATE
POWER SUPPLY
NON-VOLATILE POWER-DETECT LOGIC
DRY- EFFECT
DRY+ EFFECT
PS1
15V CT @ 1.1A
BOARD 1
BOARD 2
DO NOT SCALE DRAWING
APPROVALS
DATE
SEQUENTIAL GROUP INC
3051 N. FIRST ST.
SAN JOSE, CA. 85134
TITLE
SCHEMATIC DIAGRAM
SIZE D
DRAWING NO. SD615-1,2
REV B2
SCALE: N/A
SHEET 3 OF 3
NEXT ASSY
USED ON
APPLICATION
615


SD615-1,2

| REV | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| 1 | PROTO | | |
| A | PRODUCTION | | |
| B | ECO - 219 | 850129 | PW |
| A1 | ECO-229 | 2-6-5 | PW |
| B1 | ECO-234 | 3-29-5 | TL |




| LAST | NOT USED |
|---|---|
| R108 | |
| TB102 | |
| S116 | |
| DS115 | |
| C108 | |
| D108 | |
| J109 | |
| P101 | |
| U103 | |

SEQUENTIAL CIRCUITS INC. 3051 N. FIRST ST. SAN JOSE,CA. 95134

TITLE: DESIGNATOR SCREEN

| SIZE | DRAWING NO. | REV |
|---|---|---|
| D | PP615-1 | 32 |

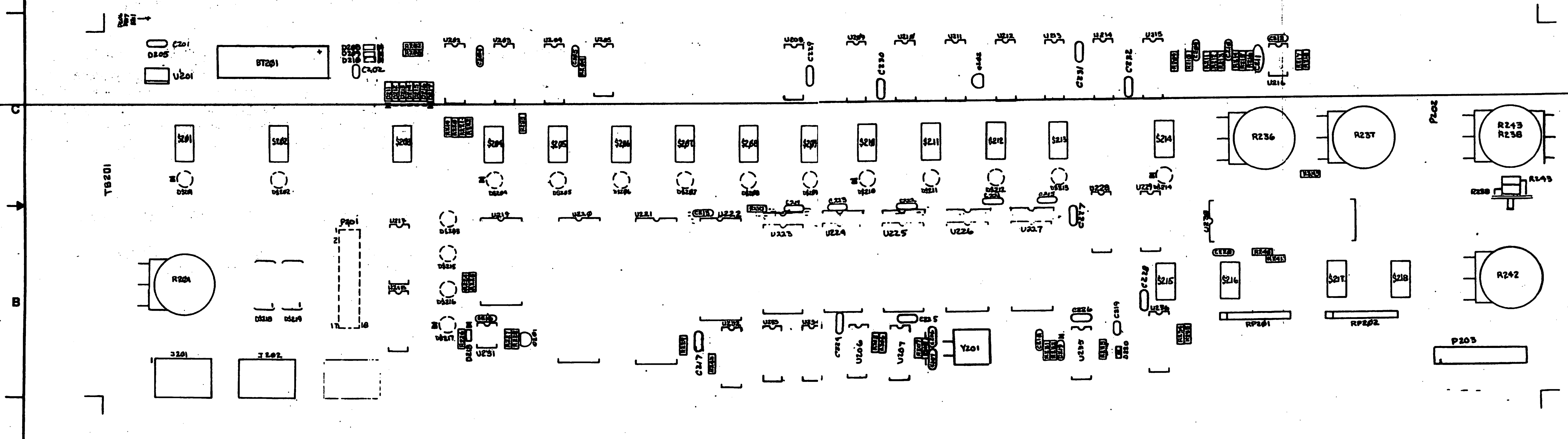
SCALE: 2:1 SHEET 1 OF 1

PP615-1

Re-order from California Reprographics

PP615-2

| REV | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| 1 | PROTO | | |
| A | PRODUCTION | | |
| B | ECO-219 | 850124 | RJ |
| B1 | ECO # 0-263 | 3-4-85 | RC |
| B2 | ECO # 294 | [illegible] | [illegible] |




| LIST | NOT USED |
|---|---|
| BT201<br>RP201<br>DS219<br>D220<br>S219<br>R245<br>C232<br>Q202<br>Y201<br>J202<br>U236<br>P203<br>TB201 | D201, 4, 6, 7<br>R209, 13, 14, 30, 31, 39, 44<br>C203, 8, 18 |

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SAN JOSE, CA. 95134

TITLE: DESIGNATOR MAP

SIZE: D | DRAWING NO.: PP 615-2 | REV: B2

SCALE: 2:1 | SHEET 1 OF 1

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|

## PARTS LIST/FUNCTIONAL DESCRIPTION

| | | | |
|---|---|---|---|
| | | Z-340 | 615 1 BOARD, ASSEMBLED |

### INTEGRATED CIRCUITS

| | | | |
|---|---|---|---|
| U101 | **+5V analog regulator** | I-428 | 780-05 |

C-1, sheet C. Regulates the +5V Analog supply. This is a +/- 1% regulator, because it is the basis of the DAC reference voltage. Power comes from +V UNREG. R103 prevents latch-up if the negative regulator powers-up first. C103 stabilizes the supply.

| | | | |
|---|---|---|---|
| U102 | **-6.5V analog regulator** | I-411 | LM7905/79M05 -5V 1A voltage regulator |

B-1, sheet C. Regulates the -6.5V required by the analog circuitry. Input is the rectified and filtered (by D105-8 and C102) 15 VAC from S101. Divider R104/105 (with filter C106) bias the reference to change the output of this regulator (normally -5V) to -6.5V. C104 filters the output.

| | | | |
|---|---|---|---|
| U103 | **+15V analog regulator** | I-405 | 78L15 15V regulator |

D-1, sheet C. Regulates the +15v Analog supply, which goes only to the DAC. Input is from voltage doubler D101/2 and C105,7.

| DESIGNATOR | SCI PART# | DESCRIPTION |
|---|---|---|
| | | **PASSIVE COMPONENTS** |
| C101 | C-075 | 3300 16V ELECT RADIAL |
| C102 | C-074 | 1000 35V ELECT RADIAL |
| C103-05 | C-105 | 47 35V ELECT RADIAL |
| C106 | C-051 | 2.2 10V 20% TANT RADIAL |
| C107 | C-105 | 47 35V ELECT RADIAL |
| C108 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| D101/02 | D-001 | 100V 1AMP 1N4002 |
| D103/04 | D-005 | 1N914 |
| D105-08 | D-001 | 100V 1AMP 1N4002 |
| J101 | J-099 | 5 PIN 240 DEGREE RT ANG PC MNT DIN CONN |
| J102-04 | J-100 | 1/4" MONO PHONE JACK LOW |
| DS101-15 | L-001 | LARGE RED TI |
| P101 | P-069 | 5 PIN LOCKING |
| R101/02 | R-243 | 10K LINEAR, REV PC |
| R103 | R-402 | 150 OHM 1/4W 5% |
| R104 | R-515 | 301 OHM 1/4W 1% |
| R105 | R-517 | 86.6 OHM 1/4 W 1% |
| R106 | R-015 | 20K 1/4W 5% |
| R107/08 | R-008 | 1K 1/4W 5% |
| S101 | S-092 | DPDT RT ANGLE PC MOUNT ROCKER SWITCH<br>Function: Power On/off switch |
| S102-16 | S-089 | OMRON KEY SWITCH<br>(used with cap, below) |

**NON-DESIGNATED COMPONENTS**

| | |
|---|---|
| S-093 | OMRON GRAY SWITCH CAP |
| S-094 | OMRON ORANGE SWITCH CAP |
| Z-338 | POWER SUPPLY HARNESS |
| J-084 | 7 PIN LOCKING HOUSING |
| P-031 | POLARIZING PINS |
| PC0615-1 | 0615 1 BOARD |

Rev B uses a jumper to connect two grounds on board.
Rev C has no mods.

## KEYBOARD SCANNER RESET PROBLEM

Units with serial number less than 100 (approximately) have an unreliable keyboard scanner reset. Sometimes, when power is first turned on, their keyboards do not work until a particular key is hit or until power is turned off and back on.

To correct this problem, simply remove C203, 10 uf 16V electrolytic, from PCB 2.

| DESIGNATOR | FUNCTION | SCI PART # | DESCRIPTION |
|---|---|---|---|

## PARTS LIST/FUNCTIONAL DESCRIPTION

| | | | |
|---|---|---|---|
| | | Z-341 | 615 2 BOARD, ASSEMBLED |

### INTEGRATED CIRCUITS

| | | | |
|---|---|---|---|
| **U201** | **+5V digital regulator** | **I-410** | **7805** |

C-1, sheet C. U201 regulates the +5V supply for the digital circuitry. Its input is +V UNREG, which comes from the 15VAC supplied through J101 and switch S101, rectified by D105-8 and filtered by C101. D205 raises the output voltage of the regulator to 5.7V, nominal, which is dropped to 5V by D208 for +Vd, the 5V digital supply, and by D209 for +Vnv (V non-volatile). When power is off, +Vnv is supplied instead by BT201 through D210. When power is on, D210 prevents lithium battery BT201 from attempting to charge, which would be dangerous.

+V UNREG also supplies U309 (C-4, sheet E).

| | | | |
|---|---|---|---|
| **U202** | **Switch driver** | **I-275** | **4099 addressable latch** |

C-1, sheet B. Normally, Q7 of this latch is high, which activates RESET (pin 2), placing the chip in a mode where it operates as an octal demultiplexer. When strobed by -SWOUT (from U204), address buss lines A5-A7 encode the output bit (Q0-Q6) which is to go high, the remainder go low. This high output goes through a diode to activate one of the columns of the switch matrix. If a switch is closed, the high is coupled to the corresponding pin of U203, Switch data buss buffer. D211-17 prevent the outputs of U202 from being connected to each other if more than one switch is pressed.

**U203** **Switch input buffer** **I-216** **4503 hex 3-state buffer**

D-2, sheet B. The 4503 tri-state buffer is divided into two sections, which are combined (pin 1 tied to pin 15) to gate information from the switch array on to the data buss. The command from the CPU is decoded by U204 and applied to U203 as -SWIN.

One of the seven columns of the switch array having been set high by U202, the high propagates through any closed switch on the row, overriding the low normally kept on the input by one of the pull-down resistors R203 and R219-23. The pattern of switches for that column, then, is placed on the data buss while -SWIN is active.

U203 also serves as the footswitch input. Plugged in to J102, the footswitch line is normally pulled up by R202. When the switch is opened or closed, the transition is smoothed by R203 and C204.

**U204** **I/O chip select decoder** **I-253** **74HC138**

A-3, sheet A. Decodes I/O chip selects to various input buffers and output latches, and stimulates the metronome (see U205-3). When A4 is high, -IOREQ is low, and -M1 is not active, an active low is present on the output corresponding to the address on pins 1-3 (A0-A2). The M1 signal is included to prevent a chip select during the Interrupt Acknowledge cycle of the Z-80A.

**U205-3,-6** **Metronome one-shot** **I-264** **74HC00 quad 2-in nand**

A-2, sheet A. A low pulse (CS) from U204-9 causes U205-6 (Metronome output) to go high. Pin 3 (and -4) immediately goes low, holding -6 high as U204-9 returns to its normally high condition. C205 gradually discharges through R204, and when it crosses the logic threshold, U205-3 goes high, forcing -6 to return low. C204 charges through R204, returning -1 to its equilibrium high. -2 remains low, keeping a high on -3 and -4 (therefore a low on -6 and -2), until the next CS pulse.

**U205-8** **Not used** **I-264** **74HC00 quad 2-in nand**

**U205-11** **Interrupt logic** **I-264** **74HC00 quad 2-in nand**

B-1, sheet B. See U235-1.

**U206-9** **Divide-by-2** **I-252** **74HC74 Dual 'D' flip-flop**

D-4, sheet A. A "T" flip-flop which converts the 8 MHz clock to a 4-MHz square wave.

| | | | |
|---|---|---|---|
| **U206-6** | **Interrupt request latch** | **I-252** | **74HC74 Dual 'D' flip-flop** |

A2, sheet B. The -Q output (-6) is normally low. If the counter interrupt mask (U215-11) is low, a -CARRY OUT signal from U210-7, programmable interrupt clock, inverted by U207-4, strobes U206-6 to a high state, placing an interrupt request on U235-3 (see U235-1). When the Z-80A acknowledges the interrupt, it executes an I/O read with A3 low and A2 high, which activates the -IORD signal from the SCI combo chip (U220-33), presetting U206-6 to the low state.

| | | | |
|---|---|---|---|
| **U207-2** | **Inverter** | **I-249** | **74HC04 hex inverter** |

A-4, sheet A. Inverts the -M1 signal from the CPU. See U204

| | | | |
|---|---|---|---|
| **U207-4** | **Inverter** | **I-249** | **74HC04 hex inverter** |

A2, sheet B. See U206-6.

| | | | |
|---|---|---|---|
| **U207-6** | **Inverter** | **I-249** | **74HC04 hex inverter** |

A3, sheet B. See U209-1.

| | | | |
|---|---|---|---|
| **U207-8** | **Inverter** | **I-249** | **74HC04 hex inverter** |

Not used.

| | | | |
|---|---|---|---|
| **U207-10** | **Inverter** | **I-249** | **74HC04 hex inverter** |

C-4, sheet A. Buffers the output of clock oscillator U207-12.

| | | | |
|---|---|---|---|
| **U207-12** | **Inverter** | **I-249** | **74HC04 hex inverter** |

D-4, sheet A. Works with Y201 8 MHz crystal, R207/8, and C206/7 as a simple RC oscillator.

| | | | |
|---|---|---|---|
| **U208** | **1.95 kHz clock divider** | **I-272** | **4040 counter** |

B3, sheet B. Divides the 500 kHz from SCI combo chip U220-19, by 256 to drive the programmable interrupt clock. (See U209.)

| | | | |
|---|---|---|---|
| **U209/10** | **Prog. interrupt clock** | **I-276** | **4029** |

B2, sheet B. The Z-80A loads the counter with the desired preset value by performing an I/O write with A4 and A3 low and A2 high. This is decoded by U233-8 and U220 to provide the -IOWR signal,

U220-34. -IOWR is inverted by U207-6 and strobes the data buss into U209/10. U209 immediately begins counting, and when the count is complete, a carry out signal from U210-7, inverted by U207-4, clocks U206-6 (if "counter mask," U215-11, is low), interrupting the CPU. This informs the CPU that it is time to advance the sequencer clock.

**U211/12** **(See passive components)**

**U213/14** **LED driver latches** **I-227** **4042 quad latch**

C-4 and D-4, sheet B. U213 and U214 together latch the eight rows of LED information from the data bus. The first section of U213 is used for D0, and the other three for D5-D7. Likewise, the first section of U214 latches D4, and the other three sections latch D1-D3. The latching is accomplished on command of -LEDOUT, from U204-13, a decoded Z-80 I/O write signal. A high is present on the data buss at this time for each LED lit in the currently active column. This high is buffered by LED drivers Q202 (for D0) and U212 (for the others), current limited by a 39 ohm resistor in U211, and applied to the anodes of the LEDs in the row. One of the columns is active, with a low on its output of U217. With this low applied to the cathode of the LED and a high on the anode, the LED lights. This column only stays lit for a few milliseconds, then the processor targets the next column, continually multiplexing the LEDs.

**U215** **Misc. output latch** **I-227** **4042 quad latch**

A-4, sheet B. Latches the first four bits of the data buss when -MISC OUT of U204-11 is strobed. Its first two outputs control the chorus on/off switch (U337-6) and the audio enable switches (U324, 25, and 27). The third output (pin 1) is the tape out, used for program, stack and sequence dumps, clock out and sync to tape. This output goes through voltage divider R209/10 and is ac coupled by C209. The output appears on J103, **To Tape.**

The fourth output of U215 is the Counter Interrupt mask. (See U206-6.)

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| U216 | **Tape comparator** | **I-301** | **311 precision comparator** |

B-1, sheet B. Converts ac-coupled data from tape into digital pulses which are read by the Z-80A through the Misc. input buffer (U229-12). With no input, R218 pulls open collector output pin 7 high. Divider R211/12 provides a bias voltage of 2.5 volts which is supplied to the reference input (pin 2) through R216. The input signal is referred to the same bias through R214 and applied to the inverting input through R215. A positive signal on the input drives the comparator output low. R217 provides hysteresis to discourage comparator oscillations during slow input transitions, and C211 also improves stability.

| | | | |
|---|---|---|---|
| U217 | **LED matrix sink** | **I-235** | **MC1413(2003)** |

B-4, sheet B. Inverts the signal from LED sink latch U218, and sinks LED current. Normally, only one output is active (low) at a time.

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| | | | |
|---|---|---|---|
| U218 | **LED sink latch** | **I-228** | **4174 hex latch** |

B-4, sheet B. Latches the LED sink data from the data buss when strobed by miscellaneous output chip select -LED SINK. The currently-active output is high, the rest are low.

| | | | |
|---|---|---|---|
| U219 | **ACIA** | **I-066** | **68A50** |

B-1, sheet A. U219 Asynchronous Communications Interface Adaptor (ACIA) converts parallel data from the CPU into serial form for transmission over MIDI, and transfers received MIDI data to the CPU.

The CPU communicates with the ACIA by means of the data buss, various address lines, and the control lines from U220 SCI Combo Chip. To write or read, the CPU sets A14 and A15 high, and A13 low, by addressing any location between C000H and DFFFH. To read, address A1, going to R/-W, is set high; it is low to write. RSEL, A0, selects the ACIA internal register. Once the address and data lines are steady, the actual data transfer occurs on the falling edge of 'E'.

Once a byte to be transmitted has been placed in the ACIA, it is shifted out TXDATA, bit by bit, one bit for every 16 TX clock pulses (pin 4). Since the TX clock is supplied by 500 kHz from U220, the bits proceed at 31.25 kBaud--the MIDI transmission rate. The TX DATA output is applied to the base of Q201 emitter follower. If the output is low, Q201 turns on, forcing current through R228, J202 pin 5, the external MIDI circuit, and back through J202, pin 4 and R227. If TXDATA is high, no current flows.

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|

Incoming MIDI data is converted from a current loop in the MIDI cable to a logic signal by U231 optoisolator, and applied to RXDATA of the ACIA. This data stream is converted to parallel form by referring it to the RX clock (pin 3).

After a byte is completely received or completely transmitted, -IREQ goes true, requesting non-maskable interrupt service from the CPU via -UINT of U220.

Since RS-232 protocols are not applicable, -RTS, -CTS, and -DCD are not used.

U220 **SCI combo chip** **I-602** **SCI combo chip**

C-3, sheet A. The combo chip decodes the CPU address and control lines to produce chip selects for the memory and input/output devices. It also measures oscillator frequencies for tuning, provides a reset pulse for the CPU, provides 'E' and 500 kHz clocks for the ACIA, and synchronizes the ACIA interrupt (see U118).

The decoding function uses inputs from address buss signals A0-A3, A14 and A15 together with CPU control signals -IOREQ, -RFSH, -MREQ, -RD and -WR. If -MREQ is active and -RFSH is not active, a memory cycle is being requested. (-RFSH active would indicate a refresh cycle, which is not used in this system.) The memory request is combined with A14 and A15 to produce chip selects.

If A14 and A15 are low, -ROM0 is selected. If A14 is high, and A15 still low, -RAM0 is selected, and if A15 is high and A14 is low, -RAM1 is enabled. If both are high, there is no chip select. (The combination of A14 and A15 high is used by other logic to select the ACIA, U124.)

The -IOREQ input of U220 is gated with A4 by U233-8. If A4 is low, the Combo chip receives an -IOREQ signal. If U220's -IOREQ input is active, -RD and -WR are combined logically with A0-A3 to produce chip selects -IOWR, -IORD, and -LATCH 0 through -LATCH 3.

The 4-MHz system clock is brought in on pin 18 and divided to produce the 500 kHz (pin 19) ACIA clock for the ACIA and the programmable interrupt clock (U209/10). -RESET (pin 25) comes from U235-10 and is fed through U220-24, -RESOUT, to the -RESET input of the Z-80A.

The TUNE input is driven by U329-7 comparator, and is connected internally to two counters which measure oscillator frequency. These counters, in turn, communicate with the CPU via the data buss (D0-D7) and the address buss.

For description of the -INT (pin 23) and -NMI (pin 22) outputs, see U221.

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| U221 | CPU | I-058 | Z-80A |

C-4, sheet A. The Z-80A microprocessor unit (CPU) runs on a 4 MHz clock from U206-9. At power on, a reset pulse is generated by U119 SCI Combo Chip (-RESOUT) that causes the CPU to begin execution at ROM location 0. The CPU places the address of a memory or I/O location on the address buss (A0-A15) and activates control signals -IOREQ, -RFSH, -MREQ, -RD, and -WR to command external devices to either place data on the data buss (D0-D7) or take it off. -M1 is used to protect against spurious I/O chip selects during the Z-80A interrupt acknowledge cycle (see U204). -BUSAK, -HALT, and -WAIT are not used. -BUSRQ is used only for factory testing, so it is pulled up with R229.

Interrupt inputs -INT and -NMI are important signals in the system. -INT (from U235-1), is the combination of three interrupts: -KEYINT from U230 Keyboard Processor, the COUNT COMPLETE signal from U209/10 Programmable interrupt clock, and a 7-millisecond timeout produced by a timer in U220 SCI Combo Chip. When answering an interrupt, the CPU polls -MISC IN (see U228-11, 13) to determine where the interrupt came from.

The -KEYINT signal tells the CPU that the Keyboard scanner has data ready. The CPU then reads the information from the scanner. (See -KEYDATA, U228/29-1.)

The COUNT COMPLETE signal from the programmable interrupt clock (via U206-6) is used to time sequencer events. When the countdown is complete, the CPU, in response to the interrupt, advances the sequencer to the next event, then presets U209/10, programmable interrupt clock, to the interval desired to the next interrupt. Provision is made for this interrupt to be masked separately (U215-11), so the CPU can prioritize the several interrupts.

The 7 millisecond interrupt paces those CPU operations which must be done regularly, such as calculating the next value for envelopes and LFOs and updating sample/holds.

-NMI comes from U219-7 -IREQ to U220 SCI Combo Chip -UINT where it is synchronized with the system clock. From there it is applied to -NMI (pin 17). It occurs when U219 ACIA either has received a byte from MIDI or has finished transmitting and is ready for another byte.

All functions that are not done on interrupts are accomplished in a "background loop". Typically the CPU spends about 4½ milliseconds responding to the 7 millisecond interrupt, leaving about 2½ milliseconds for background processing before the next interrupt.

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| U222 | **Operating firmware** | Z-1064 | **MULTI-TRAK software 2-1** |

D-3, sheet A. Contains the operating firmware for the CPU. Address and data busses are connected to the CPU, and the CPU reads the data by pulling -OE low (active) through decoded -ROM0 output of U220 SCI Combo Chip. Although use of -CE for the chip select would save power, this method allows use of a slower EPROM.

| | | | |
|---|---|---|---|
| U223-27 | **Non-volatile RAM** | I-043 | 6116 LP-4 |

D-1,-2, and-3, sheet A. These RAMs provide scratchpad storage and non-volatile program, sequence, and stack storage for the Z-80A. To either read (-OE) or write (-WE), the chip select must be enabled through U232 and one of the OR gates U233/34.

| | | | |
|---|---|---|---|
| U228/29 pins 3-9 | **Data buss buffers** | I-216 | **4503 hex 3-state buffer** |

B-4, sheet C. These tri-state buffers are enabled by the Z-80A (through -KEYDATA from U204-7) when it wants to read data from the keyboard scanner (U230).

| | | | |
|---|---|---|---|
| U228/29 (11,13) | **Misc. input buffer** | I-216 | **4503 hex 3-state buffer** |

B-1, sheet B. These tri-state buffers are enabled by -MISC IN from I/O chip select decoder U204. The signals gated on to the data buss are from the ADC and tape comparators, from -KEYINT, and from COUNT COMPLETE.

| | | | |
|---|---|---|---|
| U230 | **Keyboard scanner** | I-612 | **Masked 68B01** |

D-4, sheet C. The keyboard scanner is a single-chip, 8-bit microcomputer with internal RAM and masked ROM. Its sole function is to scan the dual-contact keyboard and convert the key closure information to key on and off and velocity data for the Z-80A CPU. When it detects that a key has been closed or opened (and velocity has been calculated), it interrupts the Z-80A using -KEYINT (pin 12, pulled up by R241), and places a byte of data on output port 3. When the CPU responds, strobing -KEYDATA to read from the data buss buffers (U228/29), the strobe is also picked up on U230-39, SC1, and the scanner then places the next byte on the output port and interrupts the CPU again, until all the bytes in the message have been transferred. For a 'key on' message, two bytes are sent; key number and velocity. For 'key off,' just the key number byte is sent. The scanner then resumes scanning the keyboard until another key event is detected.

The keyboard scanning is conducted by applying a high signal to one column at a time of keyboard matrix W1, by advancing Column Enable decoded counter U236 using a clock from U230-8 (P20). Each

key, it can be seen, has two contacts. The inner contacts are read through port 1 (pins 13-20), and the outer ones through port four (pins 30-37). When a closure is detected on the inner contact, the current reading of an internal free-running counter is noted. When the outer contact of the same key closes, the noted value is subtracted from the present counter value, giving the time-of-flight of the key. This time is then converted to a velocity value using an internal look-up table, and sent to the CPU.

The 6801 comes in two speeds, 2MHz and 1 MHz. Early production has used the 1MHZ part, and a jumper on PCB 2 connects its clock input to 4MHz instead of the 8MHz indicated on the schematic.

The keyboard is continuously scanned except when the scanner is communicating with the CPU. The column enable CLOCK input (U236-14) should be (in the case of a 1 MHz 6801) an 8 kHz string of negative pulses, and the CARRY output (U230-8) should be an approximate 1 kHz square wave, except for a momentary interruption when a key is depressed or released, while the scanner is waiting for the CPU to reply to the interrupt. Absence of these pulse trains indicates that either the CPU is not responding to -KEYINT or the scanner does not recognize that the CPU is responding (-KEYDATA).

The outputs to the shift register are pulled up by R234/35, and the inputs from the matrix rows are pulled down by RP201/02. Since the internal clock oscillator is not used, pin 2 (XTAL) is grounded, and 8 or 4MHz is supplied to pin 3 (EXTAL) from U207-10. Port two bits 2 and 3 (pins 10/11) are not used. Pin 10 is pulled up through R240, and pin 11 is connected directly to +5V digital. Both interrupt inputs are unused and connected to +5V digital, as is standby Vcc (pin 21). SC2 (pin 38) is unused, as is pin 40. Output to the CPU data buss is through port 3 (pins 22-29), buffered by U228/29. The scanner is reset (pin 6) at power up by -RESET, U235-10.

**U231** **Optoisolator** **I-330** **PC-900 optoisolator**

B-1, sheet A. The current from a MIDI transmitter similar to Q201 (described under U219) comes in pin 5 of J201, through U231-2, the internal LED, through U231-1 and R226, and out J201-4. Current through the LED turns it on, and its light turns on the adjacent phototransistor (internal to U231, between pins 4 and 5), which places a low on U219-2, RXDATA. If no current is flowing, R224 pulls RXDATA high.

**U232** **Memory address decoder** **I-253** **74HC138**

B-3, sheet A. Decodes the memory chip selects for the five non-volatile RAMs, U223 through U227. When a memory request is made (-MREQ true) with A15 high and A14 low, U220 Combo chip

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|

produces a -RAM0 true, enabling U232. One of its outputs then goes low, according to the state of address buss lines A11 through A13 (pins 1-3).

Before the chip select gets to the memory chip, it is gated with the -PWR ON signal from the power on logic (see U235-4) to prevent chip selects from occurring until the power supplies have stabilized on power-up, or during power-down.

**U233-3** **NV chip select gate** **I-251** **74HC32**

C-2, sheet A. Inhibits chip selects to U223 while power is unstable. Battery powered from +Vnv. See U232.

**U233-6** **NV chip select gate** **I-251** **74HC32**

C-2, sheet A. Inhibits chip selects to U224 while power is unstable. Battery powered from +Vnv. See U232.

**U233-8** **-IOREQ gate** **I-251** **74HC32**

B-3, sheet A. Inhibits -IOREQ signal to U220 while A4 is high. (U204 is enabled when A4 is high.) Battery powered from +Vnv.

**U233-11** **NV chip select gate** **I-251** **74HC32**

C-2, sheet A. Inhibits chip selects to U225 while power is unstable. Battery powered from +Vnv. See U232.

**U234-3,-11** **OR gate** **I-251** **74HC32**

Not used.

**U234-6** **NV chip select gate** **I-251** **74HC32**

C-2, sheet A. Inhibits chip selects to U226 while power is unstable. Battery powered from +Vnv. See U232.

**U234-8** **NV chip select gate** **I-251** **74HC32**

C-2, sheet A. Inhibits chip selects to U227 while power is unstable. Battery powered from +Vnv. See U232.

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| **U235-1** | **Interrupt logic** | **I-248** | **74HC02** |

B-1, sheet B. Sums the three interrupt inputs with a logical OR function. First, the "seven millisecond" interrupt from U230-23 and the -KEYINT signal from U230-12 are combined by U205-11. An active (low) signal on either or both of them produces a high on U235-2. Completion of count by U209/10 produces a high on U235-3. A high on either of its inputs produces a low on pin 1, which goes to U221-16, -INT of the CPU. (See U221.)

| | | | |
|---|---|---|---|
| **U235-4,-10,-13** | **Power detect logic** | **I-248** | **74HC02** |

Incoming 15VAC power is full-wave rectified by D103/04, divided by R106 and R232, and filtered by C108. D219 protects inputs -5 and-6 of U235. U235 is always operational because it is supplied by Vnv from BT201 through D210. When power is first turned on, D103 or 104 detect the first wave, C108 begins to charge and, as the voltage at -5 and -6 rises past U235's logic threshold, produces a low on pin 4. Previously, pins 8 and 9 were high, because of pin 4, so pin 10 was low, making -RESET true and -PWR ON false. A low on pin 8 cannot produce a change in the output until pin 9 also goes low, after C219 charges through R233 to the low on pin 4. This charge time, which takes place after the supply has stabilized, controls the length of the -RESET signal. When -RESET goes high and -PWR ON goes low, normal operation commences.

When power is removed from the circuit, C108 discharges quickly through R232, and when the threshold is passed, U235-4 goes high, causing (through pin 8) pin 10 to go low, so -RESET is true and -PWR ON is false. -RESET stops the Z-80A and -PWR ON inhibits chip selects to non-volatile RAM (see U233 and U232), protecting RAM from involuntary erasure. D220 discharges C219 quickly so that, if power is immediately re-applied, a -RESET pulse of normal length is obtained.

| | | | |
|---|---|---|---|
| **U236** | **Keyboard Column Enable** | **I-207** | **4022 octal counter** |

A-3, sheet C. This decoded divide-by-eight counter drives the columns of the keyboard matrix. On power up, the -PWR ON signal from U235-13 resets the counter to "0." (Q0, pin 2 is high.) When the keyboard scanner (U230) has finished reading column 0, it sends a negative pulse out P20 (pin 8) to the CLOCK input of the counter, advancing it to the next count. Now Q1 (pin 1) is high. When Q0 through Q3 are high, the CARRY output (pin 12) is high, and when Q4-Q7 are high, CARRY is low. This way the scanner can read P21 to keep track of the state of the counter. (See U230.)

| DESIGNATOR | SCI PART# | DESCRIPTION |
|---|---|---|
| | | **PASSIVE COMPONENTS** |
| BT201 | E-040 | 2.9V LITHIUM BATTERY |
| C201 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C202 | C-020 | 1.0 25V 20% TANT RADIAL |
| C204/05 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C206/07 | C-065 | 20PF 10% 50V CERAMIC RADIAL |
| C209 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C210 | C-014 | .02 50V 20% DISC RADIAL |
| C211 | C-004 | 100P 50V 10% DISC RADIAL |
| C212-17 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C219 | C-051 | 2.2 10V 20% TANT RADIAL |
| C220-32 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| D205 | D-001 | 100V 1AMP 1N4002 |
| D208 | D-001 | 100V 1AMP 1N4002 |
| D209-18 | D-005 | 1N914 |
| D219 | D-008 | 1N34 |
| D220 | D-005 | 1N914 |
| DS201-17 | L-001 | LARGE RED TI LED |
| DS218/19 | L-009 | 7 SEG DISPLAY COMMON CATHODE |
| J201/02 | J-087 | 5 PIN RT ANGLE PC MNT DIN CONN |
| P201 | P-092 | 34 PIN DBL RON HEADER .930 HIGH |
| P202 | P-091 | 34PIN DBL ROW HEADER .970 |
| P203 | P-090 | 26 PIN DBL ROW .1" HEADER |
| Q201 | T-003 | PNP TRANSISTOR 2N4250 |
| Q202 | T-002 | NPN TRANSISTOR 2N3904 |
| R201 | R-243 | 10K LINEAR, REV PC |
| R202 | R-012 | 10K 1/4W 5% |
| R203 | R-025 | 100K 1/4W 5% |
| R204 | R-018 | 47K 1/4W 5% |
| R205/06 | R-010 | 2K 1/4W 5% |
| R207 | R-045 | 10M 1/4W 5% |
| R208 | R-040 | 22K 1/4W 5% |
| R210 | R-040 | 22K 1/4W 5% |
| R211/12 | R-011 | 4.7K 1/4W 5% |
| R215/16 | R-018 | 47K 1/4W 5% |
| R217 | R-061 | 4.7M 1/4W 5% |
| R218 | R-011 | 4.7K 1/4W 5% |
| R219-23 | R-040 | 22K 1/4W 5% |
| R225 | R-011 | 4.7K 1/4W 5% |
| R229 | R-025 | 100K 1/4W 5% |
| R232 | R-056 | 51K 1/4W 5% |
| R233 | R-025 | 100K 1/4W 5% |
| R234/35 | R-012 | 10K 1/4W 5% |
| R236/37 | R-243 | 10K LINEAR, REV PC |

| DESIGNATOR | SCI PART# | DESCRIPTION |
|---|---|---|
| R238 | R-246 | DUAL GANG 100K LINEAR TAPER |
| R240/41 | R-012 | 10K 1/4W 5% |
| R242 | R-010 | 2K 1/4W 5% |
| R242 | R-243 | 10K LINEAR, REV PC |
| R243 | R-246 | DUAL GANG 100K LINEAR TAPER |
| R245 | R-049 | 240 1/4W 5% |
| R224 | R-403 | 270 1/4W 5% |
| R226-28 | R-402 | 150 OHM 1/4W 5% |
| RP201/02 | R-304 | 10K X 9 SIP |
| S201-18 | S-089 | OMRON KEY SWITCH (see switch cap below) |
| TB201 | E-171 | 20 PIN RIB JUMP 3/10"W RIGHT ANGLE BENT LEAD |
| U211 | R-300 | 39 X 8 RESISTOR NETWORK |
| U212 | T-011 | TRANSISTOR CA3082 |
| Y201 | E-112 | 8 MHZ CRYSTAL |

## NON-DESIGNATED COMPONENTS

| | |
|---|---|
| J-016 | 40 PIN DIP SOCKET |
| J-045 | 28 PIN DIP SOCKET |
| M-486 | VERTICAL HEATSINK (Used on U201.) |
| S-093 | OMRON GRAY SWITCH CAP |
| S-094 | OMRON ORANGE SWITCH CAP |

| | | | |
|---|---|---|---|
| A | PRODUCTION | | |
| B | ECO-[illegible] | 850128 | [illegible] |
| B1 | REVISED PER ECO # 0-285 | 2-6-85 | [illegible] |
| B2 | REVISED PER ECO # 0-294 | 3-29-85 | [illegible] |

AUDIO SWITCHES

VOICE 1
VOICE 2
VOICE 3
VOICE 4
VOICE 5
VOICE 6

INPUT FILTER

DELAY LINE

OUTPUT FILTER

CHORUS ON/OFF SWITCH

OUTPUT DE-EMPHASIS

LFO

SINE SHAPER

DRY-EFFECT

DRY +EFFECT

INVERTER

LEVEL SHIFTER

CLOCK

TUNE ANALOG SWITCH

U326 BUFFER

SPARES:

| LAST | NOT USED |
|---|---|
| C3180 | D301-3 |
| D319 | R385 |
| R3128 | |
| U337 | U301,2 |
| J310 | |
| Q303 | C307,128,132,133 |
| TB301 | C305,6 |

NOTE:
1. THIS PART IS STUFFED WHEN 5106's ARE USED.
2. THIS PART IS NOT STUFFED WHEN 5106's ARE USED.

| | |
|---|---|
| NEXT ASSY | USED ON |
| APPLICATION | 615 |

DO NOT SCALE DRAWING

| APPROVALS | DATE |
|---|---|
| DRAWN | 2-1-84 |
| CHECKED | 6/14/84 |
| ENGR ENGR | |
| MECH ENGR | |
| MFG ENGR | |

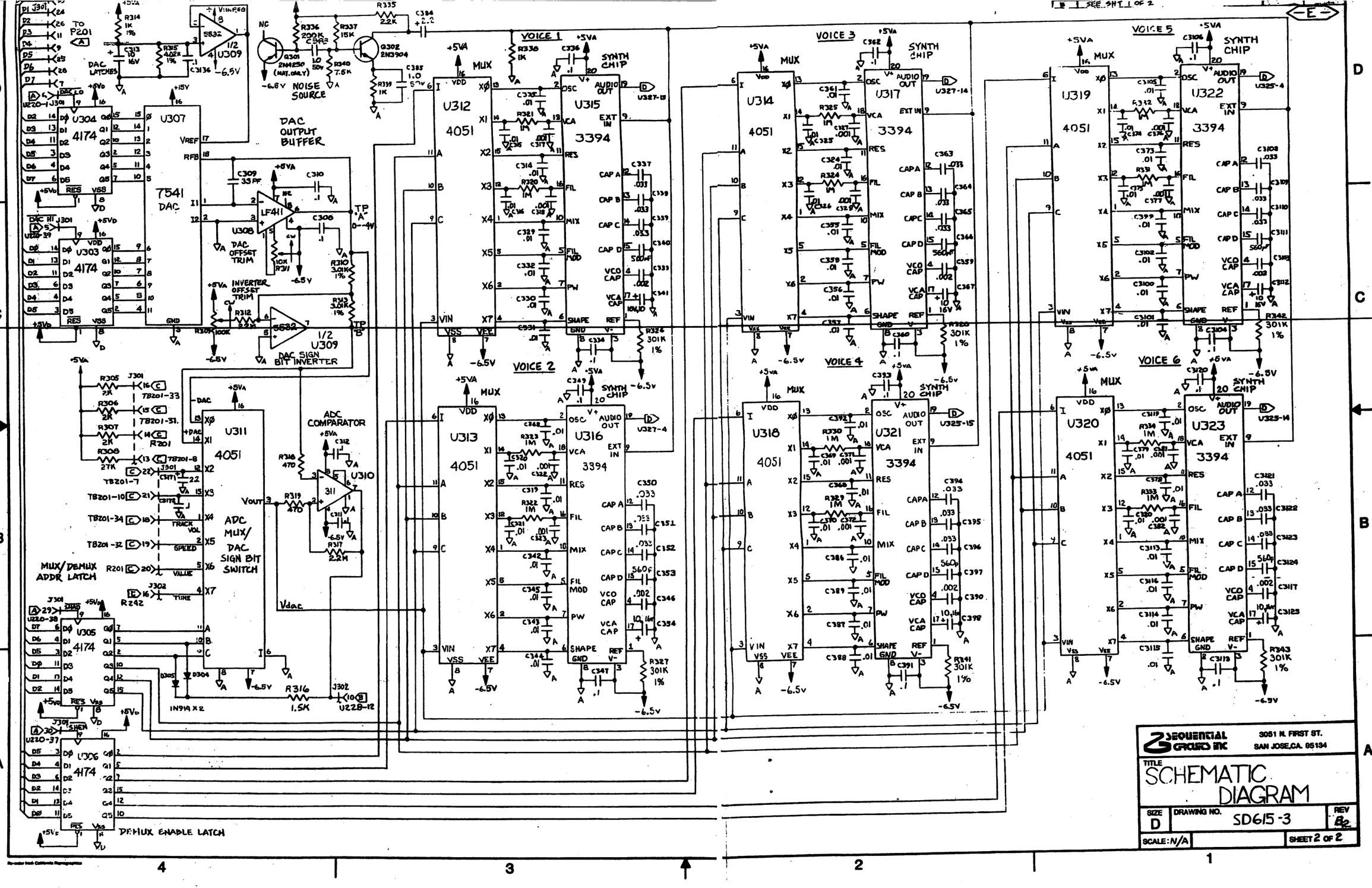
SEQUENTIAL CIRCUITS INC. 3051 N. FIRST ST. SAN JOSE, CA. 95134

TITLE: SCHEMATIC DIAGRAM ANALOG BOARD

SIZE D | DRAWING NO. SD615-3 | REV B2

SCALE: N/A | SHEET 1 OF 2

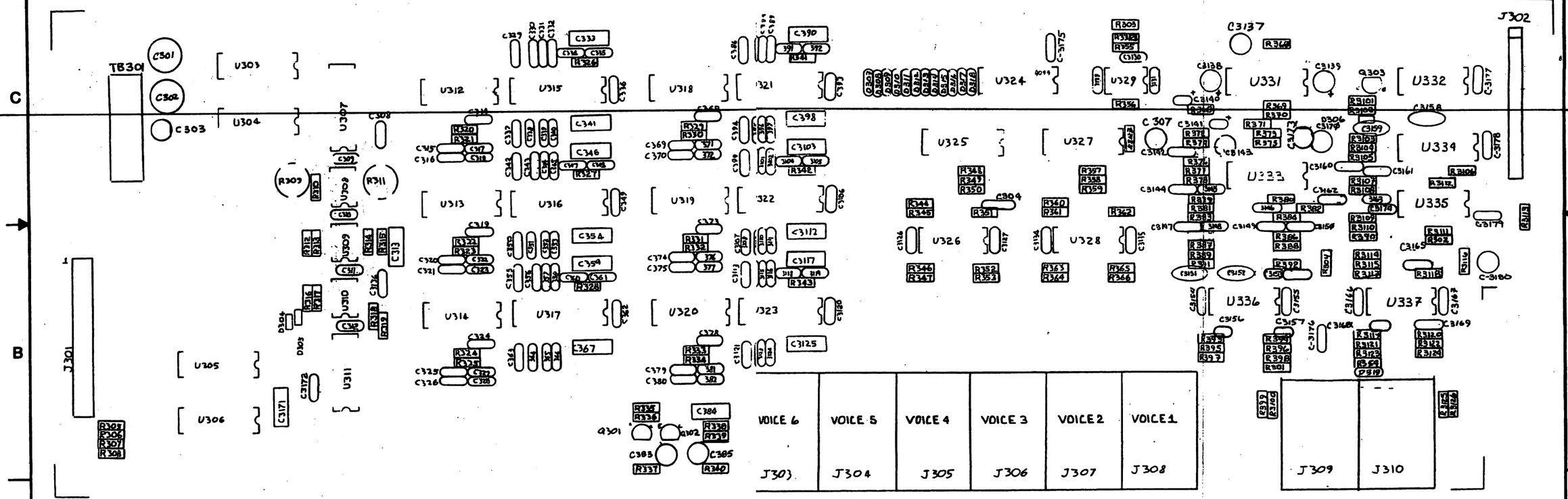
SD615-3



SEE SHT 1 OF 2
VOICE 1
VOICE 2
VOICE 3
VOICE 4
VOICE 5
VOICE 6
DAC OUTPUT BUFFER
NOISE SOURCE
DAC LATCHES
DAC OFFSET TRIM
INVERTER OFFSET TRIM
DAC SIGN BIT INVERTER
ADC COMPARATOR
ADC MUX/ DAC SIGN BIT SWITCH
MUX/DEMUX ADDR LATCH
DEMUX ENABLE LATCH
SYNTH CHIP
MUX
SEQUENTIAL GROUPS INC
3051 N. FIRST ST.
SAN JOSE, CA. 95134
TITLE
SCHEMATIC DIAGRAM
SIZE D
DRAWING NO. SD615-3
REV B2
SCALE: N/A
SHEET 2 OF 2


SD615-3

| | | | |
|---|---|---|---|
| 1 | PROTO | | |
| A | PRODUCTION | | |
| B | ECO - 219 | 850124 | PW |
| B1 | REVISED PER ECO #0-229 | 2-6-85 | PW |
| B2 | [illegible] | 3-29-85 | [illegible] |




| LAST | NOT USED |
|---|---|
| C3180 | D301, 3 |
| D319 | R385 |
| R3128 | U301, U302 |
| U337 | C3107, 128, 132, 133 |
| J310 | C305, 6 |
| Q303 | |
| TB301 | |

| | |
|---|---|
| | 615 |
| NEXT ASSY | USED ON |
| APPLICATION | |

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES
TOLERANCES: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH

DO NOT SCALE DRAWING

| APPROVALS | DATE |
|---|---|
| DWN DRAFTING | 12-84 |
| CHECKED | |
| ELEC ENGR | |
| MECH ENGR | |
| MFG ENGR | |

SEQUENTIAL CIRCUITS INC
3051 N. FIRST ST.
SAN JOSE, CA. 95134

TITLE: DESIGNATOR MAP

SIZE D | DRAWING NO. PP 615-3 | REV B2

SCALE: NA | SHEET 1 OF 1

PP615-3

Re-order from California Reprographics

## DAC TRIM

See Figure 2 for location of trimmers and test points.

1. Warm-up 615 (with cover closed) for at least five minutes.

2. Hold **Program Record** and press **PROGRAM/PARAMETER 7.** This sets the DAC output to 0V to allow you to measure the DAC offset. (This also locks-up the computer so that to reset will require switching power off/on.)

3. Use a 3½ digit DVM with a 100 millivolt full scale range and 0.05% accuracy or better.

4. On PCB 3, connect DVM to TPA and trim R311 DAC offset for a reading of 0V +/- 0.1 millivolt.

5. Add 1 millivolt to the reading obtained in step 4.

6. Connect DVM to TPB and trim R309 Inverter offset to the value figured in step 5, +/- 0.1 millivolt.

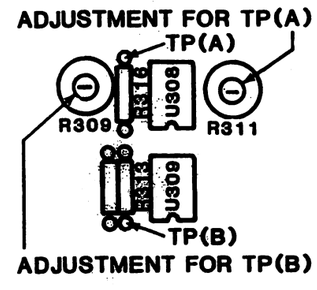



**Figure 2**
**Trimmer and Test Point Locations**

7. Seal the trimmers with latex sealer or equivalent. Do not use nail polish as it will make readjustment impossible.

Latex sealer is available from:

Techform Laboratories, Inc.
215 West 131st St.
Los Angeles, CA 90061

order Model TC-530 flexible mask and mold seal

## AUDIO OUTPUT FIELD UPDATE

Some instruments prior to S/N 684 had excessive hum and noise present on the audio output. In response to customer complaints, the following procedure should be performed under warranty. This procedure also increases the audio output volume slightly.

PARTS REQUIRED

| QUANTITY | SCI PART # | DESCRIPTION |
|---|---|---|
| 3 | C-045 | .1 uf DECOUPLING CAP |
| 1 | C-103 | 47 uf ELECTROLYTIC |
| 1 | R-047 | 10 ohm ¼ W 5% RESISTOR |
| 2 | R-068 | 100 ohm ¼ W 5% RESISTOR |
| 1 | R-014 | 15k ohm ¼ W 5% RESISTOR |
| 1" | ----- | #26 or smaller wire, Teflon insulated. |

PROCEDURE:

1. Disassemble the instrument and remove PCB 3.

2. Refer to Figure 3, Silkscreen, and perform the following steps:

   a. Remove one R-029 1M ¼ W. resistor.

   b. Replace one R-076 27K ¼ W. resistor with one R-014 15k ohm ¼ W.

3. Refer to Figure 4, Component side traces, and perform the following steps:

   a. Cut five traces

   b. Add one R-068 100 ohm ¼ W. resistor

   c. Add one R-047 10 ohm ¼ W. resistor

   d. Add one C-045 .1 uf capacitor

   e. Add one C-103 47 uf capacitor

4. Refer to Figure 5, Solder side traces, and perform the following steps:

   a. Cut one trace.

   b. Add one jump.

   c. Add two C-045 .1uf capacitors

   d. Add one R-068 100 ohm ¼ W. resistor.

5. Reassemble and perform a complete functional test.

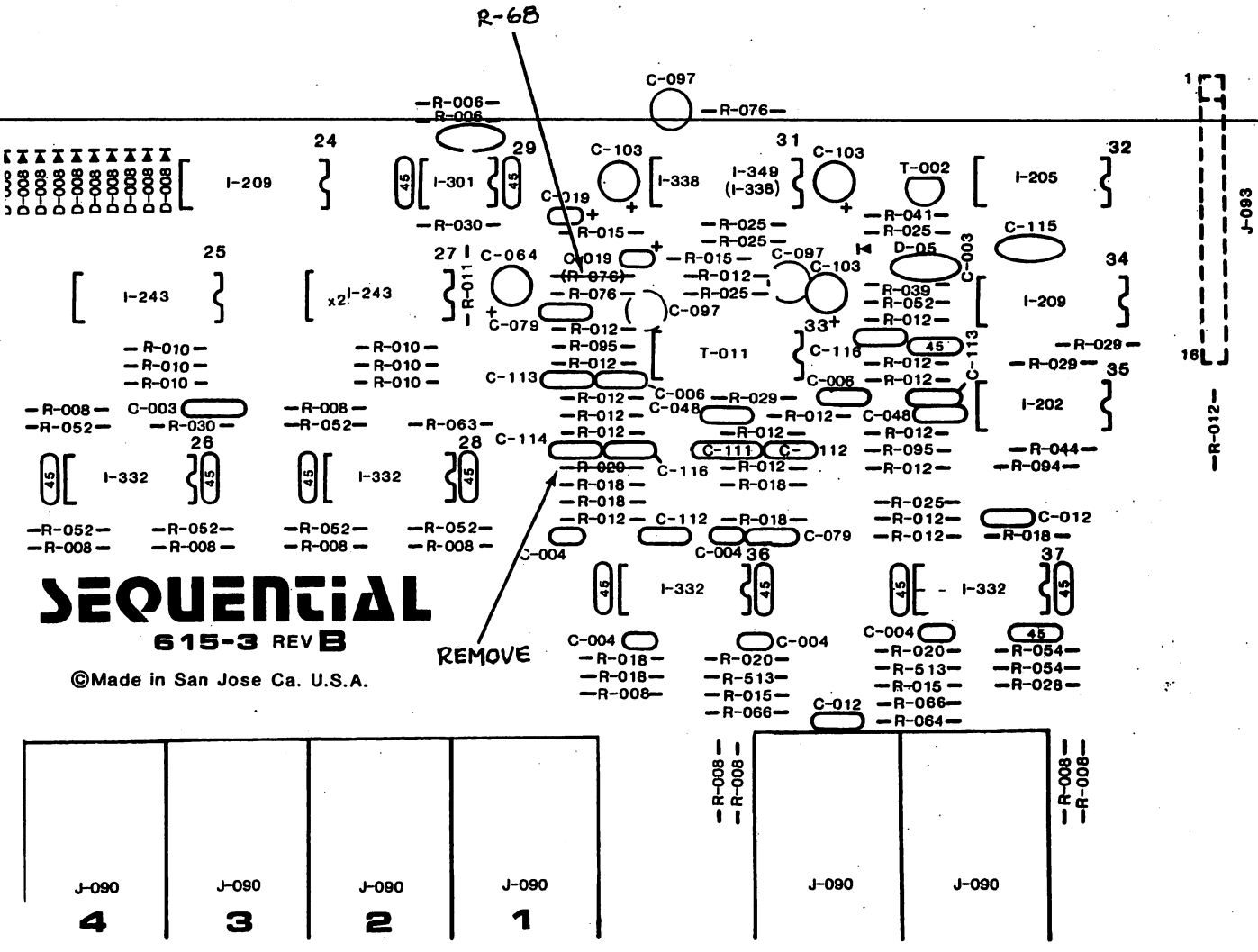



Figure 3 Silkscreen

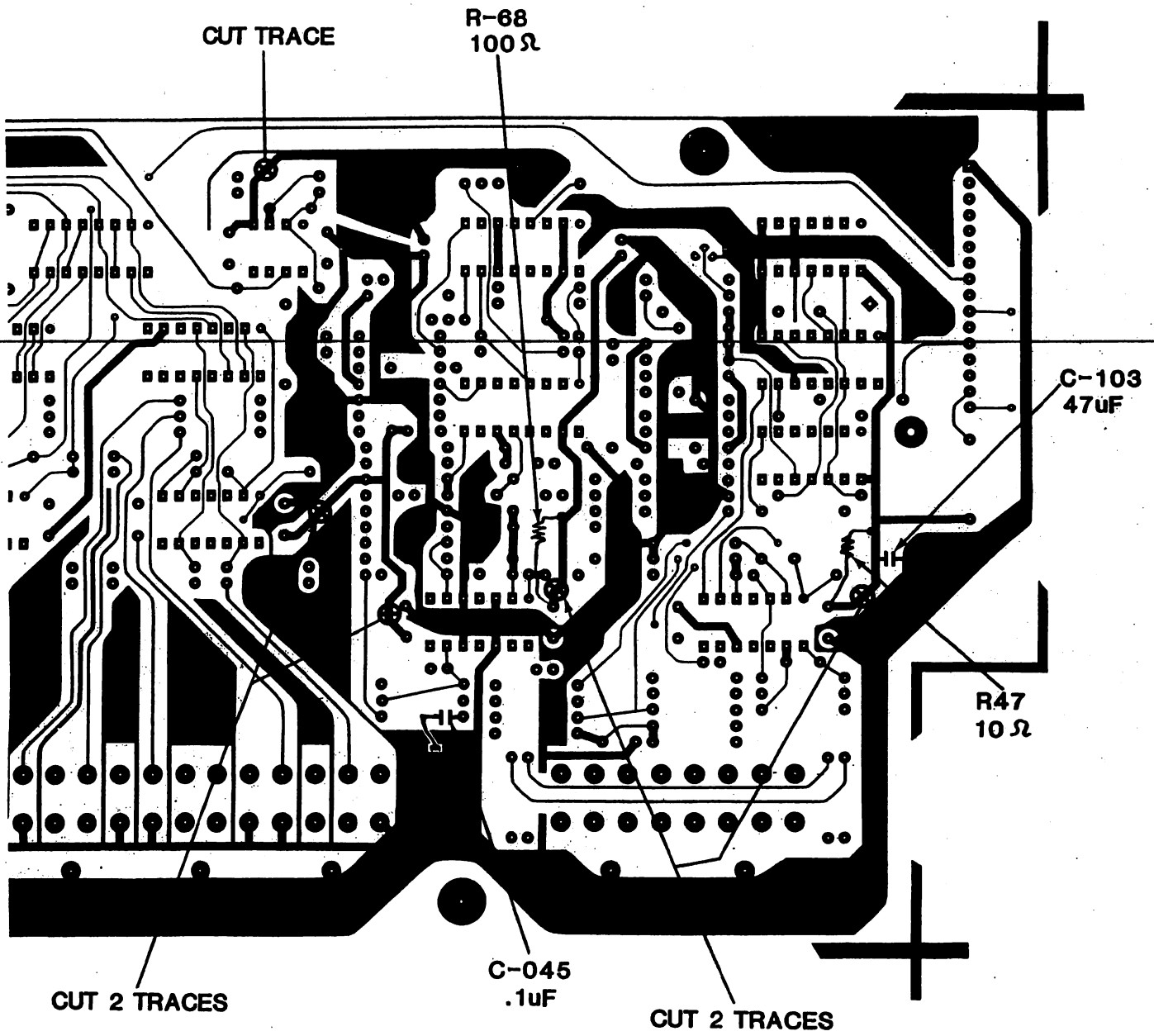



Figure 4 Component side traces

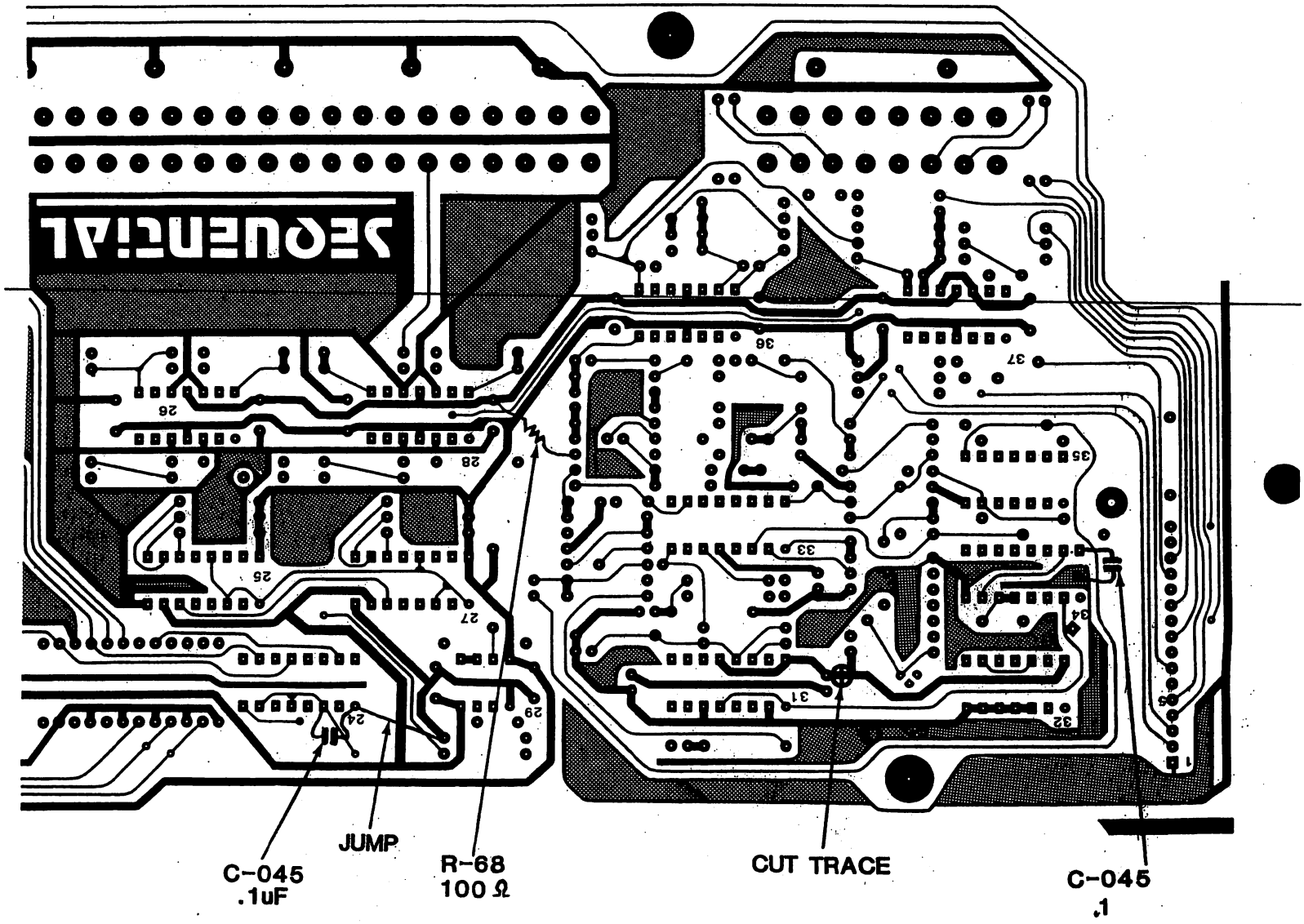



Figure 5 Solder side traces

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|

## PARTS LIST/FUNCTIONAL DESCRIPTION

Z-342 Board 3, Assembled

### INTEGRATED CIRCUITS

**U301/02** **Not used**

**U303** **DAC latch-hi** **I-228** **4174 hex latch**

C-4, sheet E. When -DAC HI, from U220 SCI combo chip, is strobed, the most significant six bits of DAC data is latched from data buss lines D0-D5.

**U304** **DAC latch-lo** **I-228** **4174 hex latch**

D-4, sheet E. When -DAC LO, from U220 SCI combo chip, is strobed, the least significant six bits of DAC data is latched from data buss lines D2-D7.

**U305** **Mux/demux address latch** **I-228** **4174 hex latch**

A-4, sheet B. This is an output latch with three functions. First of all, it holds the address of the sample/hold currently selected, on outputs Q3 (least significant), Q4, and Q5 (most significant). This data is taken from bits D0-D2 of the CPU data buss.

Secondly, the 13th, or sign bit, of the DAC is latched from CPU data buss bit 7, and goes from U305-7 to U311 address A. (See U311.)

Thirdly, the pot multiplexer address is latched from bits D5 and D6, appears on Q1 and Q2, and goes to U311-10 and -9. When a pot is selected, D304 and D305, through R316, provide a pullup voltage for the open-collector output of U310. (See U311.)

The latch strobe is -SHAD from U220 Combo Chip.

**U306** **Demux enable latch** **I-228** **4174 hex latch**

A-4, sheet E. After the DAC has had time to settle (see U305, U307), U306 selects one of the multiplexers to receive the DAC output. The selection data comes from CPU data buss bits D0-D5, is latched by the -SHEN signal (decoded by U220 SCI Combo Chip) and goes to the Inhibit lines of the multiplexers for Voices 1-6. (U312/13, U314, and U318-20, respectively.) The voice currently addressed is low and the rest are inhibited by a high on their 'I' input. The selected Sample/Hold now opens and begins to charge to the DAC voltage (see U312).

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| **U307** | **12-Bit DAC** | **I-514** | **DAC7541 (12 bit)** |

D-4, sheet E. Generates the control voltages that control the synthesizer chips. The twelve-bit word comes from latches U303/04.

The 7541 is a CMOS DAC. It gets 15-volt analog power at pin 16. The internal resistor ladder network is supplied a stable +4V reference voltage from U309-1. This voltage causes a proportional current to flow through each weighted arm of the 12-bit DAC ladder. At the other end of each arm is a current steering switch, controlled by the corresponding bit from the DAC latch. If the bit is off, the current is dumped onto current bus I2 (pin 2), which is connected to ground. If the bit is on, the current is routed to I1 (pin 1), which goes to the virtual ground inverting input of U308 DAC output amplifier (current-to-voltage converter). Inside the DAC is a feedback resistor connected from I1 to Rfb (pin 18) and U308-6. U308 produces an output voltage that drives a current through Rfb that is equal and opposite to that flowing from Vref through I1. This is the action of the op amp to keep its noninverting (pin 3, connected to ground) and inverting inputs at the same potential. Therefore, U308-6 swings from 0 to -4V.

Note that the input offset voltage of U308 must be trimmed to less than .1mV by R311. This is not because a DC output error would be any problem, but because any difference in voltage between I1 and I2 causes error currents to flow through the ladder whose effects are dependent on the pattern of bits applied to the DAC, thus causing a non-linearity in the output.

| | | | |
|---|---|---|---|
| **U308** | **DAC output amplifier** | **I-346** | **LF411** |

C-4, sheet E. See U307 for functional description. The LF411 has a high slew rate, which is useful for charging sample and hold capacitors. Its overall settling time is improved by C309, which slows down the slewing just enough to prevent overshoot and ringing.

Input offset voltage must be precisely controlled in this circuit. (See description under U307.) Input offset voltage drift with temperature, often a problem with BIFET op amps, is reduced to acceptable limits by the LF411. A BIFET is used here because input bias currents flowing through I1 of U307 can cause non-linearities similar to the problems caused by excess input offset voltage.

| | | | |
|---|---|---|---|
| **U309-1** | **DAC reference buffer** | **I-324** | **NE5532 dual op-amp** |

D-4, sheet E. Unity gain non-inverting buffer. The 4V reference is provided by divider R314/15 from +5V Analog, which is regulated to within 1% by U101. C313 provides low frequency, and C3136, high frequency, bypassing. Buffering the reference is necessary because the input impedance of U307 (VREF) is low and varies considerably

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|

from chip-to-chip. (The 3394 synthesizer voice chip requires an accurate reference.) Pin 4 of U309 is supplied with -6.5V and pin 8 has positive power supplied by +V UNREG, to provide ample headroom for the swing to +4V (see U309-7). The power supply rejection ratio of the 5532 is adequate to work with an unregulated supply.

**U309-7** **DAC inverter** **I-324** **5532 dual low noise amp**

C-4, sheet E. Inverts the 0 to -4V DAC signal from U308-6 (TPA). (See U307, U308) The result (U309-7 or TPB) is a 0 to +4V mirror image of the DAC output. One of these two outputs (TPA or TPB) is then selected by U311 as the sign, or 13th bit. Input resistor R310 and feedback resistor R313 are matched to .1% so that overall gain is -1 +/-0.1%. This means the slope of the positive portion of the output (TPB) could be different than the negative (TPA), by as much as .05%. Ordinarily, this would not do for a 13-bit DAC, but here the tune routine corrects for any long-range nonlinearity by tuning each octave. Therefore the DAC must have true 13-bit linearity only within each octave. Since the DAC can cover 10 octaves (8 volts at 3/4 volt/octave), 0.05%/10 = 0.005% or true 13-bit accuracy.

The inverter DC offset must be adjusted, with R309, to produce an output at TPB exactly 1 LSB (VREF/4096 = .976 mV) more positive than TPA, when the DAC is loaded with all zeroes. The stability of this adjustment is enhanced by the superior offset drift vs. temperature characteristic of the 5532.

**U310** **ADC comparator** **I-301** **311 precision comparator**

B-3, sheet E. When one of the pots connected to inputs X2-X7 of U311 is selected, its voltage appears on U311-3 and, through R319, on U310-2, the non-inverting comparator input. The inverting input (pin 3) is driven by the 0 to +4V DAC voltage from U309-7, through R318. When DAC voltage exceeds pot voltage, the output goes low. R317 provides hysteresis for stability. The output is pulled up by R316 (see U305) and drives pin 12 of misc input buffer U228.

**U311** **DAC sign bit switch/ ADC multiplexer** **I-211** **4051 8-in analog mux**

B-4, sheet E. If inputs B and C are low, U311 acts as a DAC sign bit switch. If control input A is low, the negative DAC signal on XO appears at VOUT. If A is high, the positive DAC signal is selected. VOUT is the final DAC signal going to all six demultiplexers (Vdac). The sign bit scheme doubles the range of the DAC, providing an effective 13th bit as well as the -4 to +4 V range required by the 3394 synthesizer voices.

If inputs B or C are high, the switch acts as a pot multiplexer (see U310). In this case the output (Vdac) from Vout to pin 3 of all the voice demultiplexers (U312, etc.), is ignored, because none of these demultiplexers are enabled.

The Inhibit input (I) is tied active low, making the switch always active. Positive and negative analog supplies are provided.

R305-8, connected to the tops of the pots, divide the pot voltage so that the maximum found on the wipers is less than the maximum DAC voltage (4V). C3171/2, on pins 12 and 15, smooth the wheel signals.

**U312** **Sample/hold demultiplexer I-211** **4051 8-in analog mux (no National)**

D-3, sheet E. Voice 1 Sample/Hold (S/H) demultiplexer.

~~On each 7 millisecond interrupt, the CPU updates all 48 S/H's, eight~~ for each of the six voices. First, voice one is updated, then voice two, etc. The following description is for voice one only--other voices work the same.

First the DAC is loaded with the CV value (see U307,-08,-09, and-11) which is converted to Vdac on U312-3, Vin. While the DAC is settling, the demultiplexer address is loaded into U305, and is applied to A, B, and C of U312, selecting one of U312's eight switches. Then 'I', U312-6, is brought low by U306-2. This strobes, or opens the selected sample and hold, completing the circuit between its capacitor (C335 for example, if A=B=C=0) and the DAC. The cap begins to charge to the DAC voltage.

After a short period, the strobe (U312-6) is shut off by the CPU (through U306) and the S/H capacitor is open circuited.

Each S/H consists of a .01 low-leakage capacitor in concert with the very high impedence of the 3394 inputs. Since there is no discharge path the capacitor retains the DAC voltage present when it was strobed, until the next strobe. Lag networks R321/C317 and R320/C318, for the VCA and filter lines respectively, smooth out 'digitation' noise which would otherwise appear on the envelopes.

**U313** **Sample/hold demultiplexer I-211** **4051 8-in analog mux (no National)**

B-3, sheet E. Voice 2 Sample/Hold (S/H) demultiplexer. (See U312.)

**U314** **Sample/hold demultiplexer I-211** **4051 8-in analog mux (no National)**

D-2, sheet E. Voice 3 Sample/Hold (S/H) demultiplexer. (See U312.)

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| U315 | **Synthesizer voice chip** | **I-336** | **CEM3394** |

D-3, sheet E. The CEM3394s are highly-integrated voltage-controlled voices which contain:

a multi-waveshape oscillator (SHAPE) with variable frequency (OSC) and pulse width (PW),
a mixer (MIX) to balance the oscillator against an external input,
a four-pole low-pass filter with adjustable frequency (FIL), and resonance (RES),
a VCA which applies the oscillator output to the filter frequency input CV (FIL MOD),
and a final VCA (VCA) which shapes the voice dynamics.

See Figure 6. CAPS A through D determine the frequencies of each filter pole. The VCO CAP sets the basic oscillator range. The VCA CAP actually ac-couples the filter output to the VCA input. R326, attached to the REF pin, sets basic oscillator range.

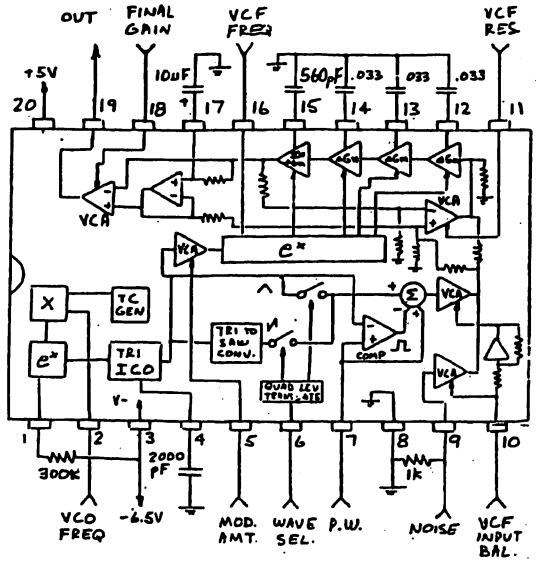



**Figure 6**
**3394 BLOCK DIAGRAM**

The external audio input of all voices is driven by Q301 noise source and amplifier Q302. C384 ac-couples the noise to the 3394s, and R338 serves as an output load.

Voice audio outputs, pin 19, go to switches U327 (for audio) and U324 (for feedback to the CPU for the tune routine).

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| **U316** | **Synthesizer voice chip** | **I-336** | **CEM3394** |
| | B-3, sheet E. Voice 2 synthesizer chip. (See U315.) | | |
| **U317** | **Synthesizer voice chip** | **I-336** | **CEM3394** |
| | D-2, sheet E. Voice 3 synthesizer chip. (See U315.) | | |
| **U318** | **Sample/hold demultiplexer** | **I-211** | **4051 8-in analog mux (no National)** |
| | B-2, sheet E. Voice 4 Sample/Hold (S/H) demultiplexer. (See U312.) | | |
| **U319** | **Sample/hold demultiplexer** | **I-211** | **4051 8-in analog mux (no National)** |
| | D-1, sheet E. Voice 5 Sample/Hold (S/H) demultiplexer. (See U312.) | | |
| **U320** | **Sample/hold demultiplexer** | **I-211** | **4051 8-in analog mux (no National)** |
| | B-1, sheet E. Voice 6 Sample/Hold (S/H) demultiplexer. (See U312.) | | |
| **U321** | **Synthesizer voice chip** | **I-336** | **CEM3394** |
| | B-2, sheet E. Voice 4 synthesizer chip. (See U315.) | | |
| **U322** | **Synthesizer voice chip** | **I-336** | **CEM3394** |
| | D-1, sheet E. Voice 5 synthesizer chip. (See U315.) | | |
| **U323** | **Synthesizer voice chip** | **I-336** | **CEM3394** |
| | B-1, sheet E. Voice 6 synthesizer chip. (See U315.) | | |
| **U324** | **Tune analog switch** | **I-209** | **4049 hex invtr/driver** |
| | A-4, sheet D. The 4049 is connected in an unconventional way as a FET switch. The control input, -AUDIO ENABLE, is connected to the gates of the six FET's (what would ordinarily be the inverter inputs, A-F). The output of each voice is connected to what would ordinarily be the inverter output. When -AUDIO ENABLE is high (indicating the TUNE cycle), there is a low impedance from the inverter outputs to Vss, pin 8, effectively connecting all the inputs to the inverting input of U326-1. | | |

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|

This is a current-mode switch, that is, the outputs of the 3394's are a current which is converted to a voltage by U326. The signal at the switch inputs and output should be 0V. D307-18 prevent excessive voltage swings from damaging the switch.

Note that since all 3394 outputs are tied together during tune, a defect in any of the outputs could cause them all to be out of tune. The bad voice should have no audio output. Voices can be individually tested using the **Track** audio outputs on the back panel.

**U325** **Audio switch** **I-243** **4053**

B-4, sheet D. Audio output switch for voices 4-6. A separate section is used for each voice. Inhibit input (pin 6) comes from -AUDIO ENABLE, and when high (as during the tune routine), all three sections are inhibited. When inhibit is low, the A input is connected to either the X or the Y output. On voice 4, for example, if a plug is not present in J305, U325-10 is pulled up by R350, and the input current is steered to the Y output, the summing node of U328 mixer. If a plug is present in J305, U325-10 is grounded, and the input is switched to U326-13, voice 4 output buffer.

These are current-mode switches. As with U324, the signal at the switch input and outputs should be 0V. D307-18 prevent any excessive voltage swing from damaging the switch.

**U326-1** **Tune buffer** **I-332** **084/TL074CN quad op amp**

A-4, sheet D. Current-to-voltage converter for the tune comparator input (see U324). Has very high gain so that it acts as a comparator. C304 improves overall speed by slowing down the slewing enough to diminish overshoot.

**U326-7** **Track 6 audio output buffer** **I-332** **084/TL074CN quad op amp**

B-4, sheet D. Buffer and V-to-I converter for voice 6 individual track output. Gm-setting resistor R345 was changed in early production from 2.7k to 1.2k ohms. R344 is a current limiting resistor to protect the output. For explanation of the J303 switching arrangement, see U325.

**U326-8** **Track 5 audio output buffer** **I-332** **084/TL074CN quad op amp**

B-4, sheet D. Buffer for voice 5 individual track output. See U326-7.

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| **U326-14** | **Track 4 audio output buffer** | **I-332** | **084/TL074CN quad op amp** |

C-4, sheet D. Buffer for voice 4 individual track output. See U326-7.

| | | | |
|---|---|---|---|
| **U327** | **Audio switch** | **I-243** | **4053** |

B-4, sheet D. Audio output switch for voices 1-3. See U325.

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|---|---|---|---|
| **U328-1** | **Mixer** | **I-332** | **084/TL074CN quad op amp** |

Sums the current outputs of all 3394's which are switched to the Y bus of U325/27. R362 sets the output level. The output of this stage becomes the dry MIX audio output, and is processed by the chorus.

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|---|---|---|---|
| **U328-7** | **Track 3 audio output buffer** | **I-332** | **084/TL074CN quad op amp** |

C-4, sheet D. Buffer for voice 3 individual track output. See U326-7.

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|---|---|---|---|
| **U328-8** | **Track 2 audio output buffer** | **I-332** | **084/TL074CN quad op amp** |

D-4, sheet D. Buffer for voice 2 individual track output. See U326-7.

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|---|---|---|---|
| **U328-14** | **Track 1 audio output buffer** | **I-332** | **084/TL074CN quad op amp** |

D-4, sheet D. Buffer for voice 1 individual track output. See U326-7.

| | | | |
|---|---|---|---|
| **U329** | **Tune comparator** | **I-301** | **311 precision comparator** |

A-3, sheet D. During the tune routine, only one oscillator at a time is operated. Its signal proceeds through U324, U326-1, and R3128 to the inverting input of U329. The non-inverting input is grounded through R353. When the oscillator signal crosses 0V, the comparator output changes polarity. The output is pulled up by R3127 and goes to U220 Combo chip, where counters under control of the CPU measure the oscillator's period. R356 adds hysteresis for stability, and C3130 is also added for stability.

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|---|---|---|---|
| **U330** | **Analog delay line** | **I-338** | **Reticon 5106 analog delay** |

C-1, sheet D. This designator is not printed on Rev B silk screens, but the location is next to U331, sharing the same 16-pin DIP hole

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|

pattern. In most models, this part is not stuffed (see U331). If it is stuffed, U331 will also be a 5106. Input is to pin 6. R371 derives a bias for pin 5, which is filtered by C3141. Pin 2, the sync input, is not used. Pin 4 is the output, and pin 1 is the square wave input which clocks the sampled signal through the stages.

**U331** **Analog delay line** **I-349** **Reticon 5107 (5106) analog delay**

D-1, sheet D. If U330 is present, both parts will be 5106's. (Two 512-stage bucket brigades.) Otherwise, U331 will be a 5107. (One 1024-stage bucket brigade.) Also, if U330 is used, R372 is removed and several other parts added, as indicated on the schematic.

R368 provides a bias for pin 5, which is filtered by C3140. The voltage at pin 5 should be about -5.8V. R369 biases the input, pin 6. C3173 capacitively couples the input. Sync, on pin 2, is not used. Pin 1 is the clock input, and pin 4 is the output. If U330 is not used, the output goes through R372 to buffer U333-7. If U330 is used, see the description under U333-4.

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**U332-1** **Not used** **I-205** **4013 dual flip-flop**

**U332-13** **Chorus clock divider** **I-205** **4013 dual flip-flop**

A-1, sheet D. Divides the chorus clock output by two. Provides a symmetrical square wave to drive the bucket brigades.

**U333-1** **Chorus input filter** **T-011** **Multiple transistor CA3082**

D-2, sheet D. Emitter follower stage. The output of U336-1 is capacitively coupled through C3164 to a three-pole low-pass filter. At the input of the filter, R3110 provides bias for the base, U333-16. R3109/C3163, R3107/C3160, and R3108/C3162 comprise the three poles of the filter, and C3160 provides positive feedback to improve damping.

The substrate of U333 is bypassed to -6.5V by C3170. (See schematic, A-2, sheet D, under "spares".)

**U333-2** **Chorus LFO sine shaper** **T-011** **Multiple transistor CA3082**

B-2, sheet D. Emitter follower stage. This stage, in concert with Q303, rounds off the peaks of the triangle wave coming in from the wiper of R236.

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| **U333-4** | **Chorus delay line buffer** | **T-011** | **Multiple transistor CA3082** |

D-1, sheet D. Emitter follower stage. If U330 is not present, U333-4 has no function.

If U330 is used, R372 is absent, and the output of U331 is coupled through input resistor R367 and coupling capacitor C3137 to the base, U333-6. The base is biased through R375 and R371. The output signal is developed across emitter resistor R373 and applied to the input, U330-6.

| | | | |
|---|---|---|---|
| **U333-7** | **Delay line output buffer** | **T-011** | **Multiple transistor CA3082** |

C-3, sheet D. Emitter follower buffering the output of the delay line. Input is from R372 or R374 (see U330/31) and coupling capacitor C3143. R370 provides bias, and R376 develops the output.

| | | | |
|---|---|---|---|
| **U333-9** | **Chorus output filter** | **T-011** | **Multiple transistor CA3082** |

C-2, sheet D. Same as input filter, U333-1.

| | | | |
|---|---|---|---|
| **U333-12** | **Chorus input buffer** | **T-011** | **Multiple transistor CA3082** |

D-3, sheet D. Emitter follower buffer. The input comes through isolation resistor R382 and coupling capacitor C3146 to the junction of base U333-11 and bias resistor R380. R384 develops the output signal, which is capacitively coupled to the input of the pre-emphasis stage, U336-1.

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|---|---|---|---|
| **U333-14** | **Not used** | **T-011** | **Multiple transistor CA3082** |

A-2, sheet D. For explanation of C3170, see U333-1.

| | | | |
|---|---|---|---|
| **U334-2** | **Chorus clock buffer** | **I-209** | **4049 hex invtr/driver** |

A-1, sheet D. Drives the bucket brigade clock inputs.

| | | | |
|---|---|---|---|
| **U334-4** | **Chorus clock buffer** | **I-209** | **4049 hex invtr/driver** |

A-1, sheet D. Drives the chorus clock divider.

| | | | |
|---|---|---|---|
| **U334-6** | **Chorus clock oscillator** | **I-209** | **4049 hex invtr/driver** |

A-1, sheet D. With U334-15, C3158, and R3111, forms a high-frequency oscillator to clock the signals through bucket brigade chips U330/31. Oscillator frequency is controlled by the LFO through one FET of U335 (pins 10-12).

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| **U334-10** | **Chorus on/off switch buffer** | **I-209** | **4049 hex invtr/driver** |

B-2, sheet D. Boosts the chorus on/off signal from level shifter U337-8 so that it goes rail-to-rail, to completely turn off switch U335-8.

| | | | |
|---|---|---|---|
| **U334-12** | **Not used** | **I-209** | **4049 hex invtr/driver** |
| **U334-15** | **Chorus clock oscillator** | **I-209** | **4049 hex invtr/driver** |

A-2, sheet D. See U334-6.

| | | | |
|---|---|---|---|
| **U335-6,7,8** | **Chorus on/off switch** | **I-202** | **4007 dual comp pair and inverter.** |

B-2, sheet D. When U334-10 is high (Chorus off), the FET is on, providing a low impedance path between C307 and -6.5V, effectively shunting the output of the delay line.

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|---|---|---|---|
| **U335-11,12** | **Chorus clock VC FET** | **I-202** | **4007 dual comp pair and inverter** |

A-2, sheet D. The resistance between pins 11 and 12 of the FET determines the frequency of the bucket brigade clock (see U334-6), and is determined by the voltage on the gate, pin 10, from the LFO sine shaper.

| | | | |
|---|---|---|---|
| **U336-1** | **Chorus pre-emphasis** | **I-332** | **084/TL074CN quad op amp** |

D-2, sheet D. The input to this stage is from C3149, capacitively coupling the output of emitter follower U333-12 in Rev B. Input network C3150/R388/R386 provides pre-emphasis, boosting the high-frequency components of the input signal to compensate for the tendency of the delay line to generate high-frequency noise. C5153 rolls off the response above the audio range.

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|---|---|---|---|
| **U336-7** | **Output de-emphasis** | **I-332** | **084/TL074CN quad op amp** |

B-2, sheet D. The output of smoothing filter U333-9 is coupled through C3147 to input resistor R387. Feedback network R389/C3152/R391 rolls off high frequencies with a curve inverse to input pre-emphasis stage U336-1. Input high frequencies passing through this stage are returned to their former levels. High-frequency noise generated in the delay line, however, suffers an overall cut, since it wasn't boosted before. C3151 provides stage stability.

| DESIGNATOR | FUNCTION | SCI PART# | DESCRIPTION |
|---|---|---|---|
| **U336-8** | **Chorus inverter** | **I-332** | **084/TL074CN quad op amp** |

B-2, sheet D. Unity gain inverter generates a delay signal for the "dry + effect" output (U337-8) that is 180 degrees out of phase with the delay signal applied to the "dry - effect" output (U336-14).

| | | | |
|---|---|---|---|
| **U336-14** | **Dry - effect output summer** | **I-332** | **084/TL074CN quad op amp** |

C-1, sheet D. Inverting summer of signals from the metronome, through R301, the dry (original) signal through R398 and R390, and the delayed signal from U336-7 via R397 and R396. Feedback resistor R394 is shunted by C3157 to improve stability. The output is passed to the top of dual-ganged Master Volume pot R238, and from its wiper through R3100 to the tip of J309 (Mix AUDIO OUTPUT A) and through R3125 to the ring of J310 (Mix AUDIO OUTPUT B).

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| | | | |
|---|---|---|---|
| **U337-1** | **Low Freq Oscillator** | **I-332** | **084/TL074CN quad op amp** |

B-3, sheet D. This is a comparator circuit, with R3118 providing positive feedback. The inverting input is referenced to ground through R3114. When the input to R3120 is above ground, the output is at the positive supply rail. The transitions are slewed by C3165, resulting in a square wave with rounded leading edges. (See U337-14.)

| | | | |
|---|---|---|---|
| **U337-7** | **Level shifter** | **I-332** | **084/TL074CN quad op amp** |

B-2, sheet D. Open-loop comparator. The non-inverting input is biased to +2.5V through R3115 and R3117. When the logic signal applied to the non-inverting signal crosses the 2.5V threshold, output pin 7 swings from one rail to the other.

| | | | |
|---|---|---|---|
| **U337-8** | **Dry + effect output summer** | **I-332** | **084/TL074CN quad op amp** |

B-1, sheet D. Similar to U336-14, except that the delay input is from inverter U336-8. The portion of the dual-ganged pot associated with this output is R243.

| | | | |
|---|---|---|---|
| **U337-14** | **Low Freq Oscillator** | **I-332** | **084/TL074CN quad op amp** |

B-3, sheet D. Integrator. (See U337-1.) The square wave output from U337-1 is fed through RATE control R237 to input resistor R3124. Depending on the size of the signal as adjusted by the rate control, output pin 14 is a ramp proceeding at a certain rate. When it crosses the threshold of comparator U337-1, the comparator's output changes polarity, and the ramp at U337-14 changes direction. The resultant output is a triangle wave, with its frequency controlled by RATE.

| DESIGNATOR | SCI PART# | DESCRIPTION |
|---|---|---|
| | | **PASSIVE COMPONENTS** |
| C301/02 | C-105 | 47 35V ELECT RADIAL |
| C303 | C-020 | 1.0 25V 20% TANT RADIAL |
| C304 | C-003 | 33P 50V 10% DISC RADIAL |
| C307 | C-064 | 2.2UF 50V NONPOLAR ELECT RADIAL |
| C308 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C309 | C-003 | 33P 50V 10% DISC RADIAL |
| C310-12 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C313 | C-095 | 10 16V 10% ELECT AXIAL |
| C314-16 | C-012 | .01 50V 20% MYLAR RADIAL |
| C317/18 | C-008 | .001 50V 10% MYLAR RADIAL |
| C319-21 | C-012 | .01 50V 20% MYLAR RADIAL |
| C322/23 | C-008 | .001 50V 10% MYLAR RADIAL |
| C324-26 | C-012 | .01 50V 20% MYLAR RADIAL |
| C327/28 | C-008 | .001 50V 10% MYLAR RADIAL |
| C329-32 | C-012 | .01 50V 20% MYLAR RADIAL |
| C333 | C-094 | .002 5% POLY AXIAL |
| ~~C334~~ | ~~C-045~~ | ~~.1 50V DECOUPLER MONO RADIAL~~ |
| C335 | C-012 | .01 50V 20% MYLAR RADIAL |
| C336 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C337-39 | C-079 | .033 100V 10% MYLAR RADIAL |
| C340 | C-007 | 560PF 50V DISC RADIAL |
| C341 | C-095 | 10 16V 10% ELECT AXIAL |
| C342-45 | C-012 | .01 50V 20% MYLAR RADIAL |
| C346 | C-094 | .002 5% POLY AXIAL |
| C347 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C348 | C-012 | .01 50V 20% MYLAR RADIAL |
| C349 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C350-52 | C-079 | .033 100V 10% MYLAR RADIAL |
| C353 | C-007 | 560PF 50V DISC RADIAL |
| C354 | C-095 | 10 16V 10% ELECT AXIAL |
| C355-58 | C-012 | .01 50V 20% MYLAR RADIAL |
| C359 | C-094 | .002 5% POLY AXIAL |
| C360 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C361 | C-012 | .01 50V 20% MYLAR RADIAL |
| C362 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C363-65 | C-079 | .033 100V 10% MYLAR RADIAL |
| C366 | C-007 | 560PF 50V DISC RADIAL |
| C367 | C-095 | 10 16V 10% ELECT AXIAL |
| C368-70 | C-012 | .01 50V 20% MYLAR RADIAL |
| C371/72 | C-008 | .001 50V 10% MYLAR RADIAL |
| C373-75 | C-012 | .01 50V 20% MYLAR RADIAL |
| C376/77 | C-008 | .001 50V 10% MYLAR RADIAL |
| C378-80 | C-012 | .01 50V 20% MYLAR RADIAL |
| C381/82 | C-008 | .001 50V 10% MYLAR RADIAL |
| C383 | C-097 | 1UF 50V ELECT RADIAL NON-POL |
| C384 | C-052 | 2.2 15V ELECT AXIAL |
| C385 | C-097 | 1UF 50V ELECT RADIAL NON-POL |
| C386-89 | C-012 | .01 50V 20% MYLAR RADIAL |
| C390 | C-094 | .002 5% POLY AXIAL |

| DESIGNATOR | SCI PART# | DESCRIPTION |
|---|---|---|
| C391 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C392 | C-012 | .01 50V 20% MYLAR RADIAL |
| C393 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C394-96 | C-079 | .033 100V 10% MYLAR RADIAL |
| C397 | C-007 | 560PF 50V DISC RADIAL |
| C398 | C-095 | 10 16V 10% ELECT AXIAL |
| C399-102 | C-012 | .01 50V 20% MYLAR RADIAL |
| C3103 | C-094 | .002 5% POLY AXIAL |
| C3104 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3105 | C-012 | .01 50V 20% MYLAR RADIAL |
| C3106 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3108-110 | C-079 | .033 100V 10% MYLAR RADIAL |
| C3111 | C-007 | 560PF 50V DISC RADIAL |
| C3112 | C-095 | 10 16V 10% ELECT AXIAL |
| C3113-116 | C-012 | .01 50V 20% MYLAR RADIAL |
| C3117 | C-094 | .002 5% POLY AXIAL |
| C3118 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| ~~C3119~~ | ~~C-012~~ | ~~.01 50V 20% MYLAR RADIAL~~ |
| C3120 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3121-123 | C-079 | .033 100V 10% MYLAR RADIAL |
| C3124 | C-007 | 560PF 50V DISC RADIAL |
| C3125 | C-095 | 10 16V 10% ELECT AXIAL |
| C3126/127 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3129 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3131 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3134-136 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3137 | C-097 | 1UF 50V ELECT RADIAL NON-POL |
| C3138/139 | C-103 | 47UF 10V ELECT RADIAL |
| C3140/141 | C-019 | .47 35V 20% TANT RADIAL |
| C3142 | C-079 | .033 100V 10% MYLAR RADIAL |
| C3143 | C-097 | 1UF 50V ELECT RADIAL NON-POL |
| C3144 | C-113 | .0033 5% MYLAR RADIAL |
| C3145 | C-006 | 470P 50V 10% DISC RADIAL |
| C3146 | C-048 | .047 50V 10% MYLAR RADIAL |
| C3147 | C-114 | .068 5% MYLAR RADIAL |
| C3148 | C-116 | .0082 10% RADIAL MYLAR |
| C3149 | C-111 | .47UF 5% MYLAR RADIAL |
| C3150 | C-112 | .0068 3% MYLAR RADIAL |
| C3151 | C-004 | 100P 50V 10% DISC RADIAL |
| C3152 | C-112 | .0068 3% MYLAR RADIAL |
| C3153 | C-004 | 100P 50V 10% DISC RADIAL |
| C3154/155 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3156/157 | C-004 | 100P 50V 10% DISC RADIAL |
| C3158 | C-115 | 68P 20% CERAMIC DISC |
| C3159 | C-003 | 33P 50V 10% DISC RADIAL |
| C3160 | C-116 | .0082 10% RADIAL MYLAR |
| C3161 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3162 | C-006 | 470P 50V 10% DISC RADIAL |
| C3163 | C-113 | .0033 5% MYLAR RADIAL |
| C3164 | C-079 | .033 100V 10% MYLAR RADIAL |
| C3165 | C-012 | .01 50V 20% MYLAR RADIAL |
| C3166/167 | C-045 | .1 50V DECOUPLER MONO RADIAL |

| DESIGNATOR | SCI PART# | DESCRIPTION |
|---|---|---|
| C3168 | C-004 | 100P 50V 10% DISC RADIAL |
| C3169 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3170 | C-103 | 47UF 10V ELECT RADIAL |
| C3171 | C-052 | 2.2 15V ELECT AXIAL |
| C3172 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3173 | C-097 | 1UF 50V ELECT RADIAL NON-POL |
| C3174 | C-048 | .047 50V 10% MYLAR RADIAL |
| C3175-79 | C-045 | .1 50V DECOUPLER MONO RADIAL |
| C3180 | C-103 | 47UF 10V ELECT RADIAL |
| D304-06 | D-005 | 1N914 |
| D307-19 | D-008 | 1N^4 |
| J301 | J-080 | 34 PIN PC MOUNT DBL ROW SOCKET |
| J302 | J-093 | 16 PIN 1" PC MNT RECEPTICLE |
| J303-10 | J-090 | 1/4" STEREO JACK W/SWTON |
| Q302/03 | T-002 | NPN TRANSISTOR 2N3904 |
| R301 | R-066 | 300K 1/4W 5% |
| R302 | R-094 | 180K 1/4K 5% |
| R303/4 | R-047 | 10 1/4 W 5% |
| R305-07 | R-010 | 2K 1/4W 5% |
| R308 | R-076 | 27K 1/4W 5% |
| R309 | R-217 | 100K 1 TURN TOP ADJUST<br>Inverter offset trimmer |
| R310 | R-164 | 3.01K 1/4W 1%<br>matched to within .1% of R313. |
| R311 | R-218 | 10K 1 TURN TOP ADJUST<br>DAC offset trimmer |
| R312 | R-030 | 2.2M 1/4W 5% |
| R313 | R-164 | 3.01K 1/4W 1%<br>matched to within .1% of R310. |
| R314 | R-008 | 1K 1/4W 5% |
| R315 | R-500 | 4.02K 1/4W 1% |
| R316 | R-009 | 1.5K 1/4W 5% |
| R317 | R-030 | 2.2M 1/4W 5% |
| R318/19 | R-006 | 470 1/4W 5% |
| R320-25 | R-029 | 1M 1/4W 5% |
| R326-28 | R-115 | 301K 1/4W 1% |
| R329-34 | R-029 | 1M 1/4W 5% |
| R335 | R-034 | 2.2K 1/4W 5% |
| R336 | R-026 | 200K 1/4W 5% |
| R337 | R-014 | 15K 1/4W 5% |
| R338/39 | R-008 | 1K 1/4W 5% |
| R340 | R-037 | 7.5K 1/4W 5% |
| R341-43 | R-115 | 301K 1/4W 1% |
| R344 | R-008 | 1K 1/4W 5% |

| DESIGNATOR | SCI PART# | DESCRIPTION |
|---|---|---|
| R345/46 | R-052 | 1.2K 1/4W 5% |
| R347 | R-008 | 1K 1/4W 5% |
| R348-50 | R-010 | 2K 1/4W 5% |
| R351 | R-030 | 2.2M 1/4W 5% |
| R352 | R-052 | 1.2K 1/4W 5% |
| R353 | R-008 | 1K 1/4W 5% |
| R354 | R-066 | 300K 1/4W 5% |
| R355 | R-006 | 470 1/4W 5% |
| R356 | R-030 | 2.2M 1/4W 5% |
| R357-59 | R-010 | 2K 1/4W 5% |
| R360 | R-008 | 1K 1/4W 5% |
| R361 | R-052 | 1.2K 1/4W 5% |
| R362 | R-063 | 910 1/4W 5% |
| R363 | R-052 | 1.2K 1/4W 5% |
| R364 | R-008 | 1K 1/4W 5% |
| R365 | R-052 | 1.2K 1/4W 5% |
| R366 | R-008 | 1K 1/4W 5% |
| R367 | R-076 | 27K 1/4W 5% |
| R368 | R-015 | 20K 1/4W 5% |
| ~~R369/70~~ | ~~R-025~~ | ~~100K 1/4W 5%~~ |
| R371 | R-015 | 20K 1/4W 5% |
| R372 | R-014 | 15K 1/4W 5% |
| R373 | R-012 | 10K 1/4W 5% |
| R374 | R-014 | 15K 1/4W 5% |
| R375 | R-025 | 100K 1/4W 5% |
| R376 | R-012 | 10K 1/4W 5% |
| R377 | R-095 | 330K 1/4W 5% |
| R378/79 | R-012 | 10K 1/4W 5% |
| R380 | R-029 | 1M 1/4W 5% |
| R381-84 | R-012 | 10K 1/4W 5% |
| R385 | R-029 | 1M 1/4W 5% |
| R386 | R-012 | 10K 1/4W 5% |
| R387-89 | R-018 | 47K 1/4W 5% |
| R390/91 | R-012 | 10K 1/4W 5% |
| R392/93 | R-018 | 47K 1/4W 5% |
| R394 | R-020 | 62K 1/4W 5% |
| R395 | R-018 | 47K 1/4W 5% |
| R396 | R-167 | 52.3K 1/4W 1% |
| R397 | R-008 | 1K 1/4W 5% |
| R398 | R-015 | 20K 1/4W 5% |
| R399/100 | R-008 | 1K 1/4W 5% |
| R3101 | R-041 | 150K 1/4W 5% |
| R3102 | R-025 | 100K 1/4W 5% |
| R3103 | R-039 | 18K 1/4W 5% |
| R3104 | R-052 | 1.2K 1/4W 5% |
| R3105 | R-012 | 10K 1/4W 5% |
| R3106 | R-029 | 1M 1/4W 5% |
| R3107-109 | R-012 | 10K 1/4W 5% |
| R3110 | R-095 | 330K 1/4W 5% |
| R3111 | R-044 | 270K 1/4W 5% |
| R3112 | R-029 | 1M 1/4W 5% |
| R3113 | R-012 | 10K 1/4W 5% |

| DESIGNATOR | SCI PART# | DESCRIPTION |
|---|---|---|
| R3114 | R-025 | 100K 1/4W 5% |
| R3115 | R-012 | 10K 1/4W 5% |
| R3116 | R-068 | 100 1/4 W 5% |
| R3117 | R-012 | 10K 1/4W 5% |
| R3118 | R-018 | 47K 1/4W 5% |
| R3119 | R-020 | 62K 1/4W 5% |
| R3120 | R-054 | 33K 1/4W 5% |
| R3121 | R-167 | 52.3K 1/4W 1% |
| R3122 | R-054 | 33K 1/4W 5% |
| R3123 | R-015 | 20K 1/4W 5% |
| R3124 | R-028 | 470K 1/4W 5% |
| R3125/126 | R-008 | 1K 1/4W 5% |
| R3127 | R-011 | 4.7K 1/4W 5% |
| R3128 | R-006 | 470 1/4W 5% |
| TB301 | P-093 | 7 PIN RT ANGLE LOCKING MOLEX |

**NON-DESIGNATED COMPONENT**

| | | |
|---|---|---|
| | J-082 | 20 PIN DUAL INLINE SOCKET |