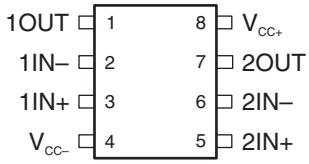
DUAL LOW-NOISE OPERATIONAL AMPLIFIERS

FEATURES

- **Equivalent Input Noise Voltage: 5 nV/√Hz Typ at 1 kHz**
- **Unity-Gain Bandwidth: 10 MHz Typ**
- **Common-Mode Rejection Ratio: 100 dB Typ**
- **High DC Voltage Gain: 100 V/mV Typ**
- **Peak-to-Peak Output Voltage Swing 26 V Typ With $V_{CC\pm}$ = ±15 V and R_L = 600 Ω**
- **High Slew Rate: 9 V/μs Typ**

NE5532, NE5532A . . . D, P, OR PS PACKAGE
SA5532, SA5532A . . . D OR P PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The NE5532, NE5532A, SA5532, and SA5532A are high-performance operational amplifiers combining excellent dc and ac characteristics. They feature very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are compensated internally for unity-gain operation. These devices have specified maximum limits for equivalent input noise voltage.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – P	Tube of 50	NE5532P	NE5532P
			NE5532AP	NE5532AP
	SOIC – D	Tube of 75	NE5532D	N5532
		Reel of 2500	NE5532DR	
		Tube of 75	NE5532AD	N5532A
		Reel of 2500	NE5532ADR	
	SOP – PS	Reel of 2000	NE5532PSR	N5532
			NE5532APSR	N5532A
–40°C to 85°C	PDIP – P	Tube of 50	SA5532P	SA5532P
			SA5532AP	SA5532AP
	SOIC – D	Tube of 75	SA5532D	SA5532
		Reel of 2500	SA5532DR	
		Tube of 75	SA5532AD	SA5532A
		Reel of 2500	SA5532ADR	

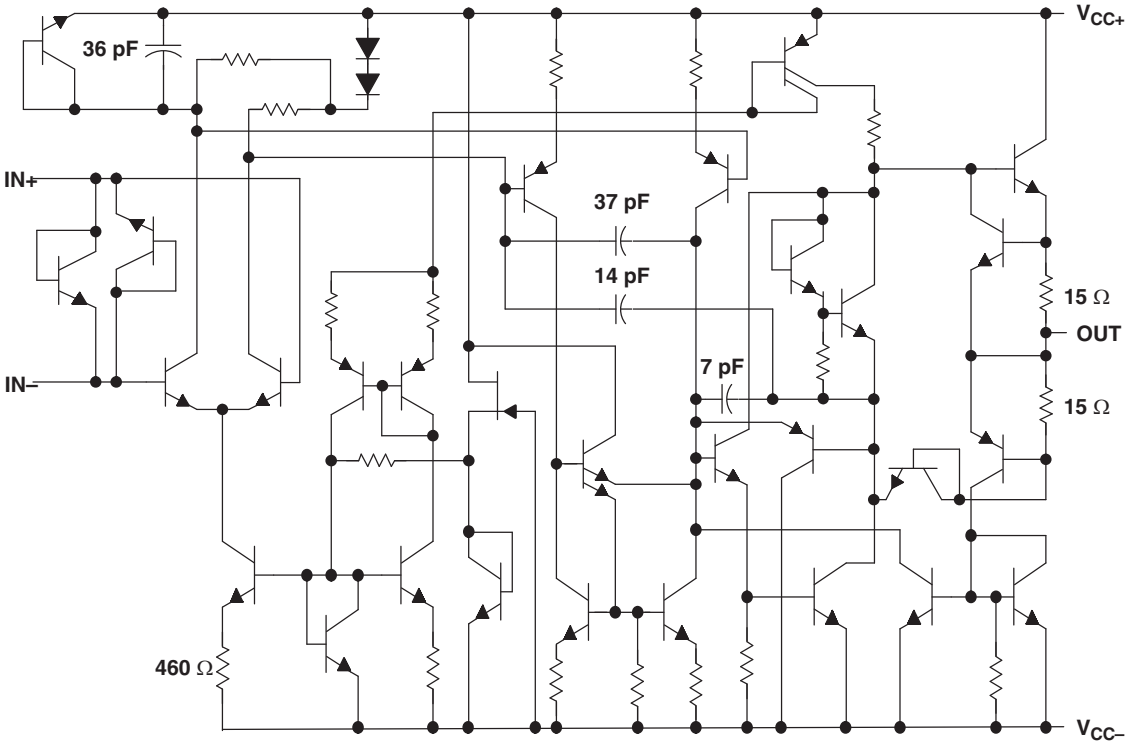
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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SCHEMATIC (EACH AMPLIFIER)



Component values shown are nominal.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage(2)	V_{CC+}	22 V
		$V_{CC–}$	–22 V
	Input voltage, either input(2)(3)		$V_{CC±}$
	Input current(4)		±10 mA
	Duration of output short circuit(5)		Unlimited
θ_{JA}	Package thermal impedance(6)(7)	D package	97°C/W
		P package	85°C/W
		PS package	95°C/W
T_J	Operating virtual-junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
(4) Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
(5) The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.
(7) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

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RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}	Supply voltage		–5	–15	V
T_A	Operating free-air temperature	NE5532, NE5532A	0	70	°C
		SA5532, SA5532A	–40	85	

ELECTRICAL CHARACTERISTICS

$V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	T_A = 25°C		0.5	4	mV
			T_A = Full range(2)			5	
I_{IO}	Input offset current	T_A = 25°C			10	150	nA
		T_A = Full range(2)				200	
I_{IB}	Input bias current	T_A = 25°C			200	800	nA
		T_A = Full range(2)				1000	
V_{ICR}	Common-mode input-voltage range			±12	±13		V
V_{OPP}	Maximum peak-to-peak output-voltage swing	R_L ≥ 600 Ω, $V_{CC\pm}$ = ±15 V		24	26		V
A_{VD}	Large-signal differential-voltage amplification	R_L ≥ 600 Ω, V_O = ±10 V	T_A = 25°C	15	50		V/mV
			T_A = Full range(2)	10			
		R_L ≥ 2 kΩ, V_O±10 V	T_A = 25°C	25	100		
			T_A = Full range(2)	15			
A_{vd}	Small-signal differential-voltage amplification	f = 10 kHz			2.2		V/mV
B_{OM}	Maximum output-swing bandwidth	R_L = 600 Ω, V_O = ±10 V			140		kHz
B_1	Unity-gain bandwidth	R_L = 600 Ω, C_L = 100 pF			10		MHz
r_i	Input resistance			30	300		kΩ
z_o	Output impedance	A_{VD} = 30 dB, R_L = 600 Ω, f = 10 kHz			0.3		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min		70	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		80	100		dB
I_{OS}	Output short-circuit current			10	38	60	mA
I_{CC}	Total supply curent	V_O = 0, No load			8	16	mA
	Crosstalk attenuation (V_{O1}/V_{O2})	V_{01} = 10 V peak, f = 1 kHz			110		dB

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
(2) Full temperature ranges are: –40°C to 85°C for the SA5532 and SA5532A, and 0°C to 70°C for the NE5532 and NE5532A.

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OPERATING CHARACTERISTICS

$V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	NE5532, SA5532			NE5532A, SA5532A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain			9			9		V/µs
	Overshoot factor	V_I = 100 mV, R_L = 600 Ω, A_{VD} = 1, C_L = 100 pF		10			10		%
V_n	Equivalent input noise voltage	f = 30 Hz		8			8	10	nV/√Hz
		f = 1 kHz		5			5	6	
I_n	Equivalent input noise current	f = 30 Hz		2.7			2.7		pA/√Hz
		f = 1 kHz		0.7			0.7		

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
NE5532AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532AIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		
NE5532AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5532AP	Samples
NE5532APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5532AP	Samples
NE5532APSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532APSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		
NE5532P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5532P	Samples
NE5532PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE5532P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
NE5532PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
SA5532AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	Samples
SA5532ADE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		Samples
SA5532ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	Samples
SA5532ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	Samples
SA5532ADRE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		Samples
SA5532ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	Samples
SA5532AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5532AP	Samples
SA5532APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5532AP	Samples
SA5532D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532	Samples
SA5532DE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		Samples
SA5532DG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		Samples
SA5532DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532	Samples
SA5532DRE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		Samples
SA5532DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532	Samples
SA5532P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5532P	Samples
SA5532PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA5532P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

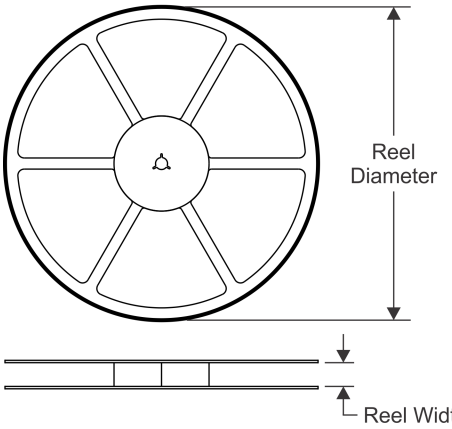
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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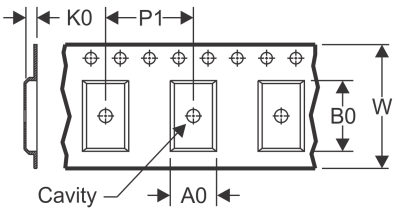
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

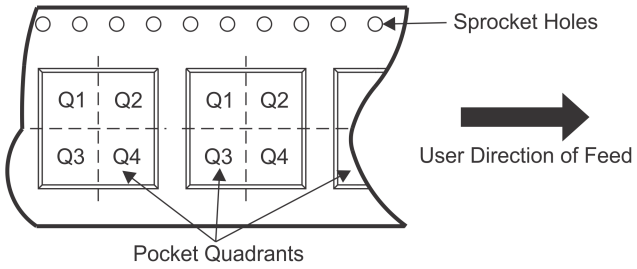


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

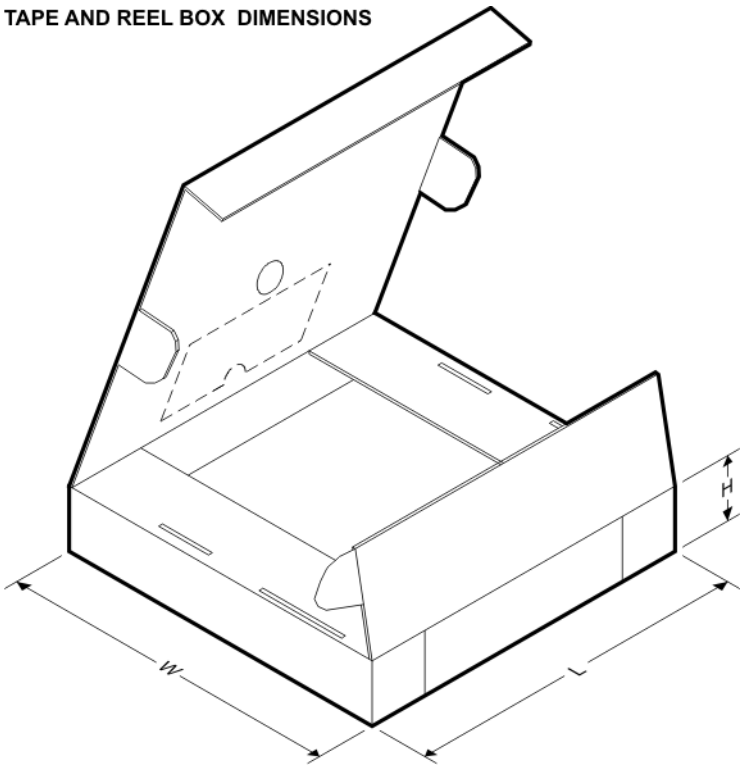
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NE5532ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532APSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
NE5532DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
NE5532DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SA5532ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5532DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

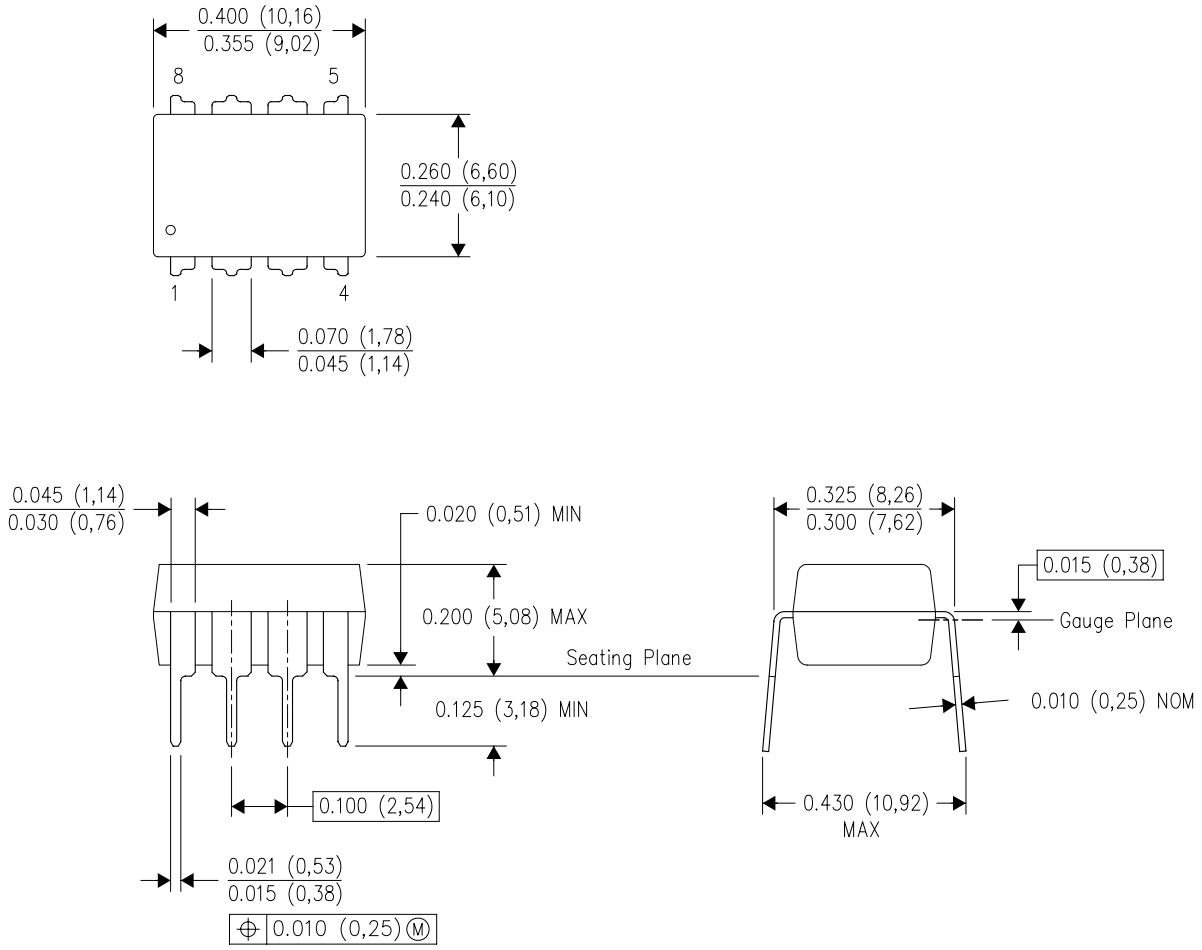
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

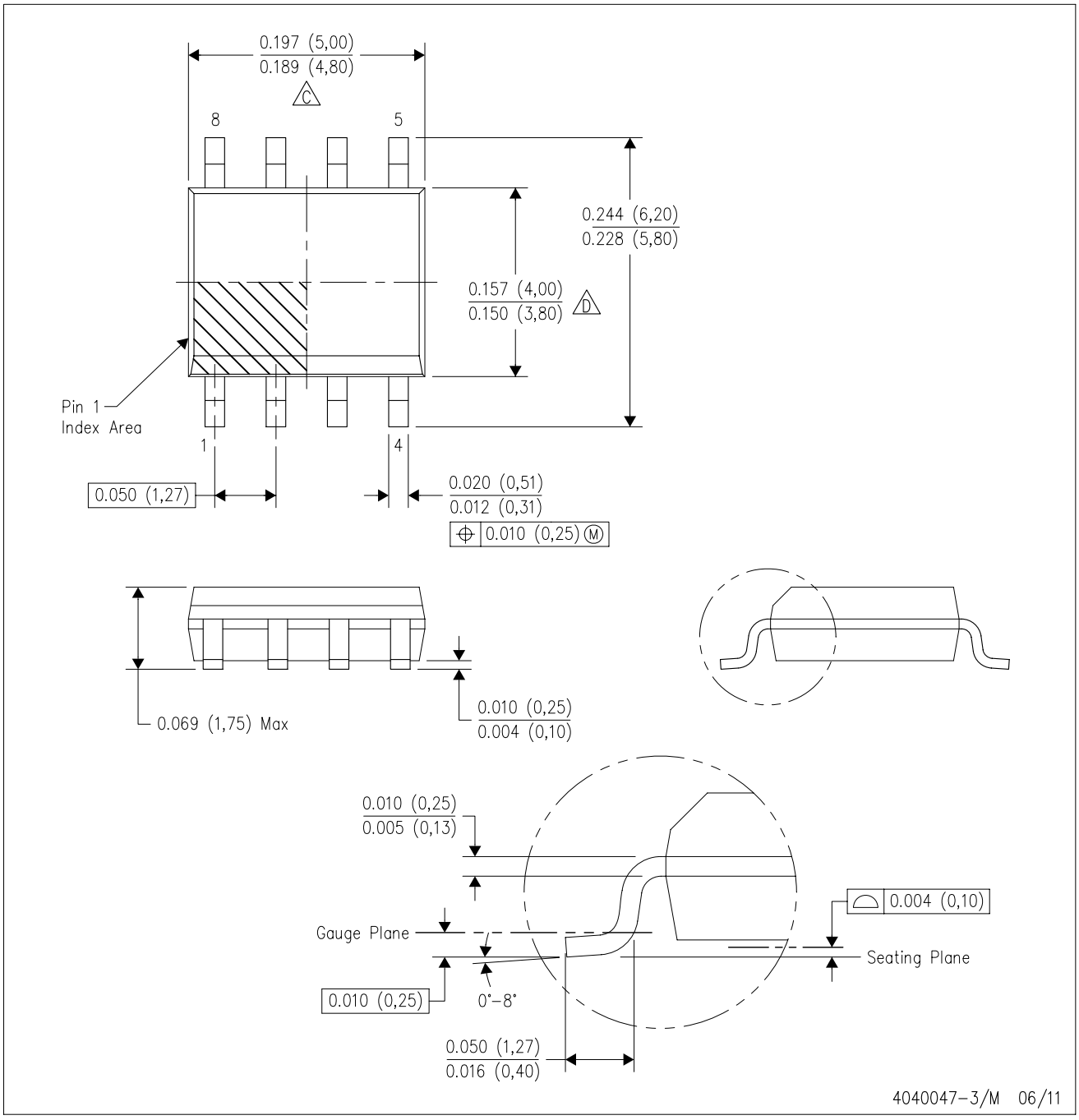
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NE5532ADR	SOIC	D	8	2500	340.5	338.1	20.6
NE5532APSR	SO	PS	8	2000	367.0	367.0	38.0
NE5532DR	SOIC	D	8	2500	364.0	364.0	27.0
NE5532DR	SOIC	D	8	2500	340.5	338.1	20.6
NE5532DRG4	SOIC	D	8	2500	340.5	338.1	20.6
NE5532PSR	SO	PS	8	2000	367.0	367.0	38.0
SA5532ADR	SOIC	D	8	2500	340.5	338.1	20.6
SA5532DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



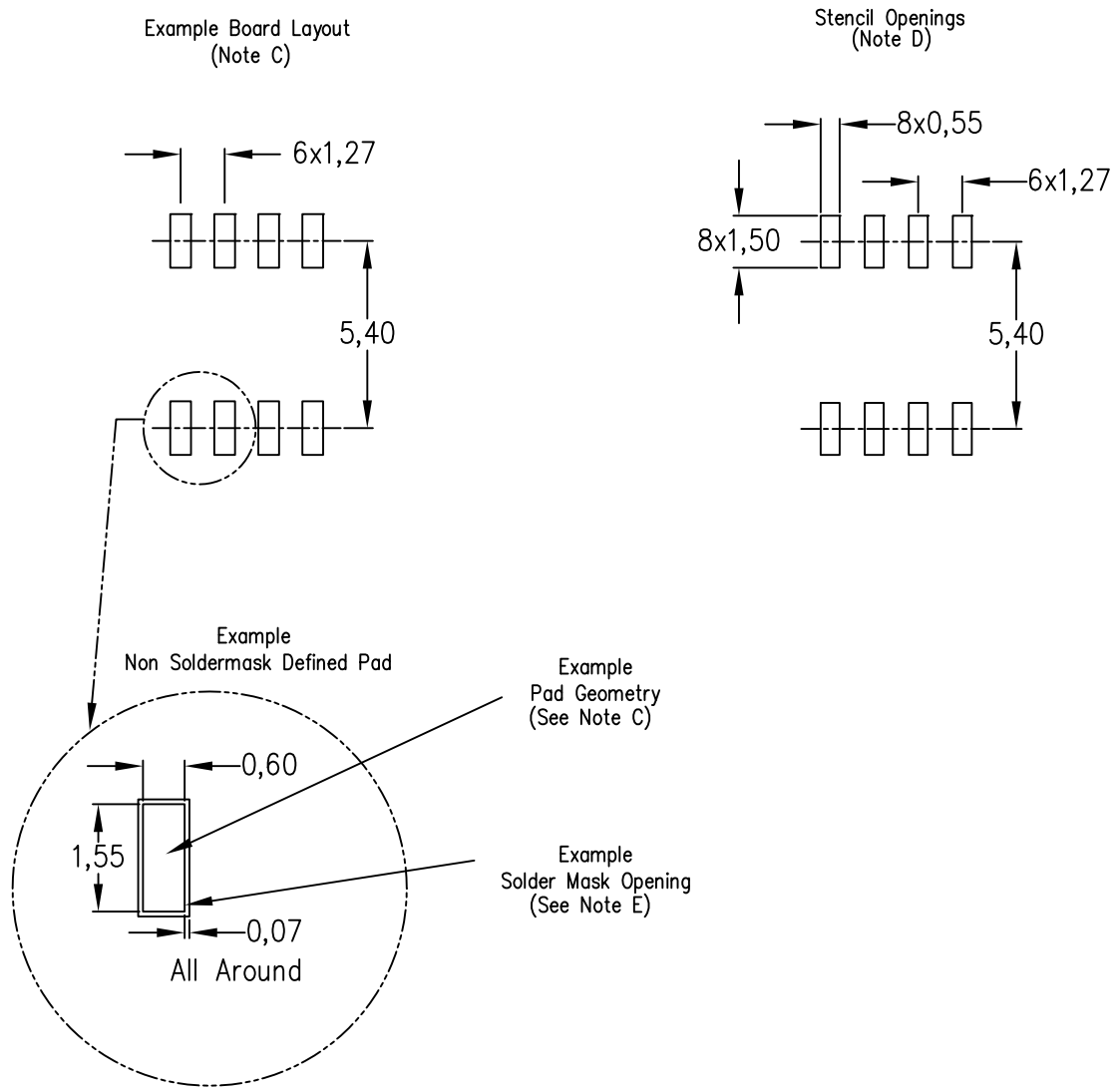
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

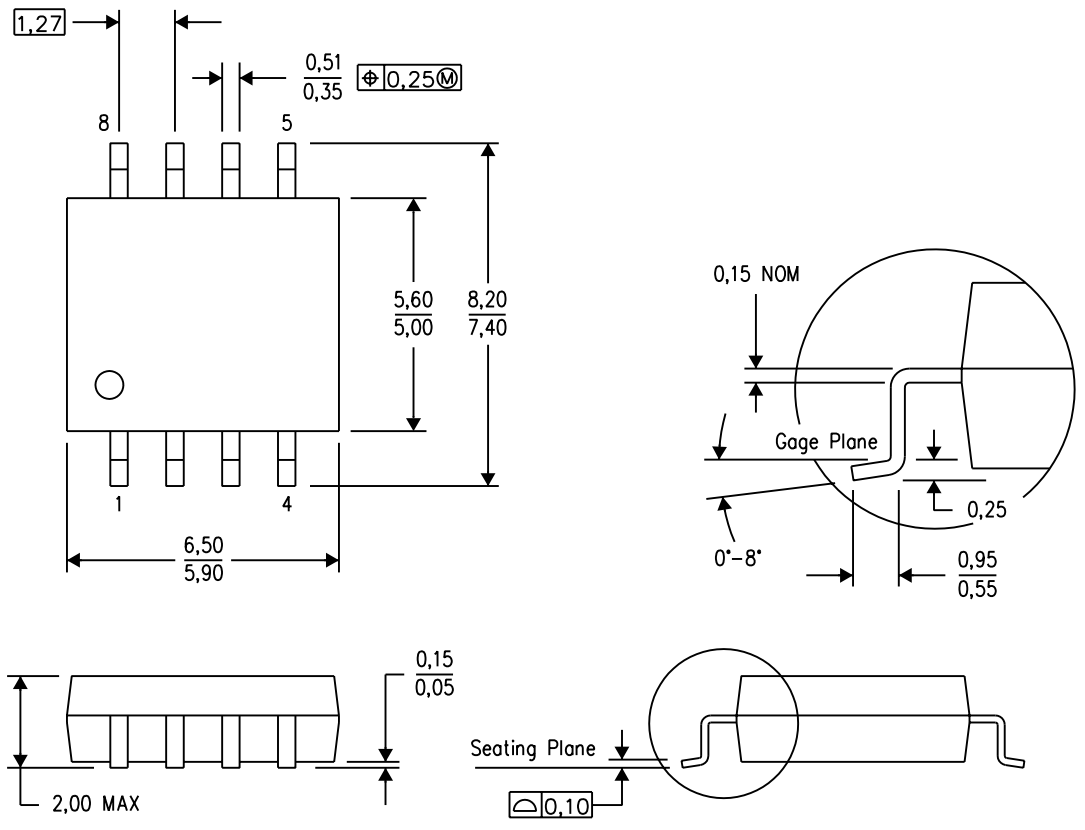
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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