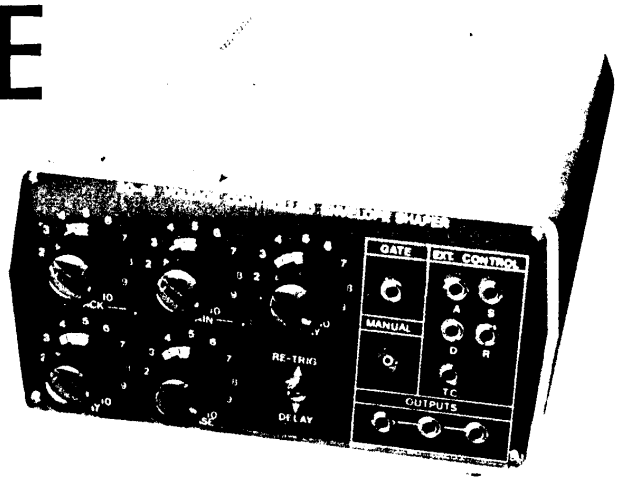
ENVELOPE SHAPER

Is it Mantovani or a Project 80 synthesiser? You can't tell the difference with this VCES designed by R.C. Blakey



Conventional ADSR envelope generators are adequate for most practical purposes since they are capable of providing a reasonable simulation of the amplitude envelopes of many musical instruments. The Project 80 Voltage Controlled Envelope Shaper (VCES) is provided for those who wish to obtain more realistic simulation or to obtain dynamic control over envelope shape. It is also a useful tool for innovative synthesis. The design incorporates the following features; bending of the standard exponential attack, decay and release curves to other shapes; alteration of attack, decay and release times by an external voltage thus allowing the envelope to be altered in proportion to the note played; the use of non linear sustain, built-in timer for re-triggering to create dual peak envelopes and also the generation of a delayed AD envelope.

Design and Application

The VCES is based on the CEM 3310 Voltage Controlled Envelope Generator produced by Curtis Electromusic Specialties. While it is well suited for use as a conventional ADSR envelope generator for both monophonic and polyphonic synthesisers the facilities provided on chip also make it ideal for configuring a complex envelope generator. The attack (A), decay (D), and release (R) parameters have a scale sensivity of 60 mV/decade (18 mV/octave) while sustain level (S) is linearly proportional to the voltage applied to pin 9. To facilitate generation of complex shapes each of the four inputs has been buffered by an op amp configured as a summer and our standard 0 to +10 V control voltages allow the A, D and R times to be varied from 2 mS to greater than 20 S. Likewise for the sustain input a voltage of 0 to +10 V varies the sustain level from 0 to 100% of the peak attack voltage which has also been normalised to +10 V.

The A, D and R responses follow an exponential curve. These characteristic curves may easily be altered in this design by taking a proportion of the output from the module and feeding it back to the appropriate input for the attack curve. The greater the amount of feedback the more convex the response and, although the overall time constant will increase, this may be adjusted over a wide range with the manual control provided. If the output is inverted prior to feedback then the attack curve will become concave in shape. Some of these curves are closer approximations to conventional instruments while others offer some novel responses. The shape of the decay curve, or the release curve, may be similarly altered and thus the VCES offers virtually unlimited scope for generation of envelope shapes. The use of low frequency waveforms to modify the time constants is also practical but setting up to obtain useful results is quite time consuming. Two attenuators, with or without inversion, are provided and the 80-5 Processor module may be used for distribution and attenuation when more complex patching is required.

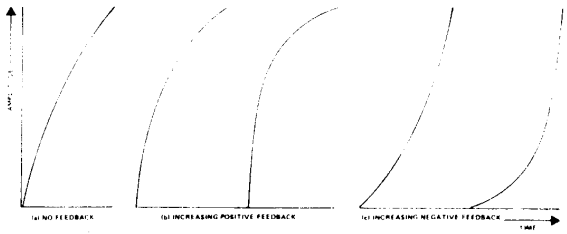


Fig.1. The effect of feedback on the attack response.

Tremolo

The sustain level also has provision for external control and one application is to apply a low frequency waveform to this input in combination with an attenuator and perhaps the manual control to produce a varying sustain. If this envelope is now used to control a VCA the effect is a tremelo only during the sustain part of the note. In the design both the upper and lower levels of the sustain control have been clamped for protection.

Another application for voltage control of envelope shape is the automatic alteration of the time constants or sustain level while the instrument is being played.

Time and Time Again

A simple timer has been incorporated in the design which allows re-triggering, or initial trigger delay, for periods up to about 2.5 S. The effect of re-triggering is to produce an envelope with two peaks, which is a transient effect exhibited by a number of conventional instruments. Often, however, as such instruments reach their peak output the

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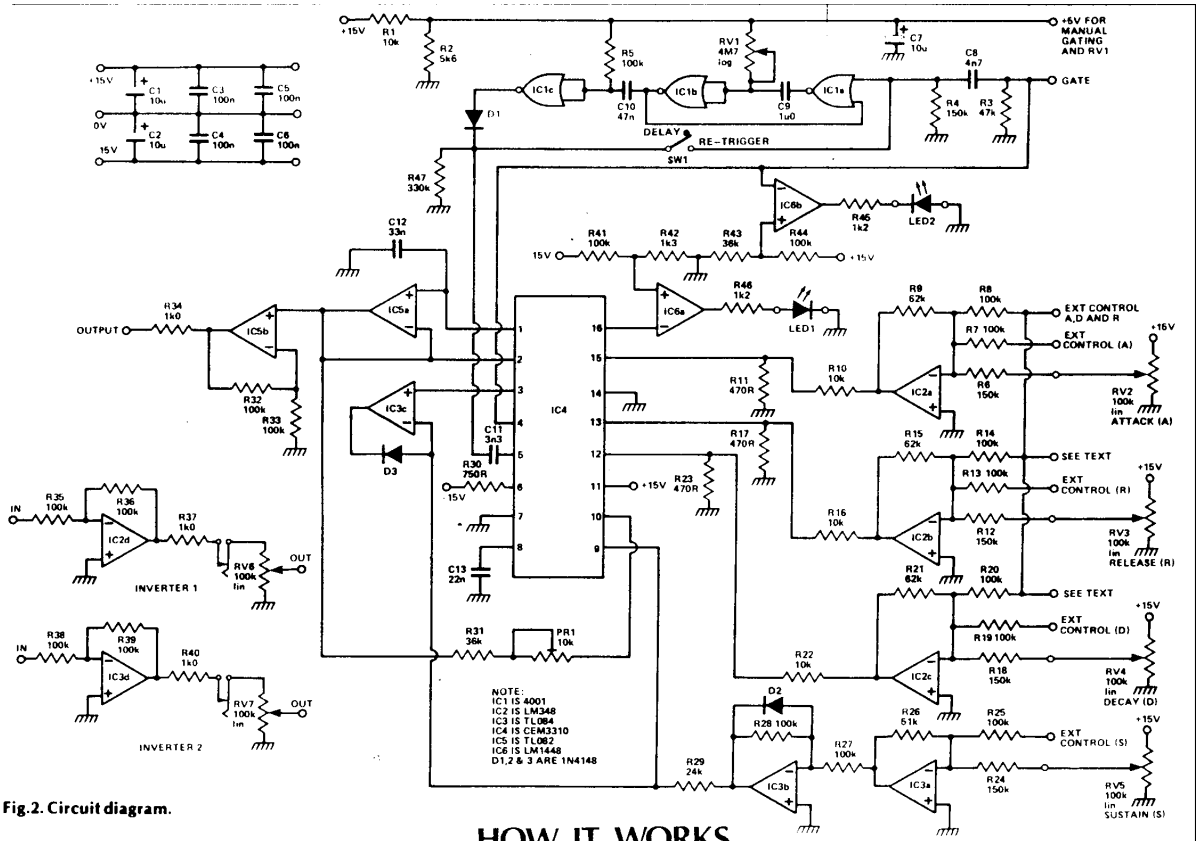


Fig.2. Circuit diagram.

HOW IT WORKS

The attack, decay and release control inputs (pins 15, 12 and 13 respectively) have a control sensitivity of 18 mV/octave and a 10k/470R attenuating network is place ahead of these inputs. The time constants of the attack, decay and release curves are determined by RxCx times the exponential multiplier, exp. (−Vc/Vt); where Rx is R31 plus part of PR1; Cx = C12; Vc = the control voltage at the appropriate pin; and Vt = kT/q. The values of Rx and Cx have been chosen to minimise errors and to retain the very low voltage feedthrough which is a feature of the CEM 3310. With the values used an increasing negative voltage at the 10k/470R attenuator will increase the time constant and a voltage from 0 to about −5V6 will give a range of 2 mS to 20 S for each time control input. To obtain both external and manual control of the time constants an inverting summer with a nominal gain of 0.62 has been placed ahead of the attenuating resistors; in the case of the attack control, using IC2a and associated resistors R6 to R9 ahead of attenuator R10/R11. Thus increasing positive voltages up to +10 V will now give the same control range. R7,8 are for external control voltages while RV2 via R6 provides manual control over the same range. R8 is connected with R14 (release control) and R20 (decay control) such that an external voltage applied to R8 will simultaneously change all three time constants.

Sustain level on the CEM 3310 is determined by the voltage at pin 9 and a voltage from 0 to +5 V will change the sustain level from 0 to 100% of the peak attack voltage. To obtain both manual and external control of sustain and retain the control polarity this input is preceded by IC3a and IC3b configured as two inverting summers with an overall gain of 0.5. Thus 0 to +10 V at R25 will produce the 0 to 100% sustain level control. Manual control is obtained with RV5 and R24. If the sustain voltage were to exceed the peak attack to 100% sustain level control. Manual control is obtained with RV5 and R24. If the sustain voltage were to exceed the peak attack voltage then the envelope will ramp up to this higher voltage level with undesirable results. Pin 3 of the CEM 3310 outputs the peak attack voltage and so the sustain level and pin 3 are connected to IC3c arranged as a precision peak follower to prevent the aforementioned situation.

The output buffer within the CEM 3310 (pin 2) has adequate drive capability for most applications but in this design it may be used to drive several inputs and overloading of the buffer will result in a loss of performance. The internal buffer has been by-passed by IC5a and the output increased to the Project 80 standard of +10 V by a non inverting amplifier, IC5b, which has a gain of two.

The attack output pin (pin 2) provides a voltage of between −0V4 and −1V2 only during the attack phase to provide a visual indication of the attack phase using LED 1. Pin 16 is connected to IC6a arranged as a comparator. IC6b is also a comparator and will turn on LED 2 when a gate voltage is present.

The CEM 3310 requires both gate and trigger pulses to generate an ADSR envelope. The 80-10 module is designed to operate with a gate voltage of +5 V and the trigger is generated by differentiating the gate pulse using C8 and R4 which is then applied to pin 5 via C11 (SW1 closed). To obtain the re-triggering and delay facilities IC1a and IC1b are used to form a monostable. The time delay is determined by the charging time of C9 via RV1 and when the voltage on C9 exceeds the threshold voltage of IC1b its output will go low and reset the monostable. IC1c is used to generate a second trigger pulse whose short duration is determined by the time required to charge up C10, to the threshold voltage level, via R5. With SW1 closed two trigger pulses are therefore generated when RV1 provides sufficient resistance to produce a noticeable delay. With SW1 open only the delayed trigger pulse is presented to pin 5 of IC4, which will allow it to operate in an AD mode.

To operate the CEM 3310 from ± 15 V supplies it is necessary to place a series current limiting resistor on the negative supply line to pin 6. The value of R20 has been chosen to comply with the general equation $R_{ET} = (V_{EE} - 7.2)/0.010$. For the timer a nominal +5 V is derived from the voltage divider formed by R1,2 since power supply to IC1 is not critical. These latter components may be changed to suit other gate voltages.

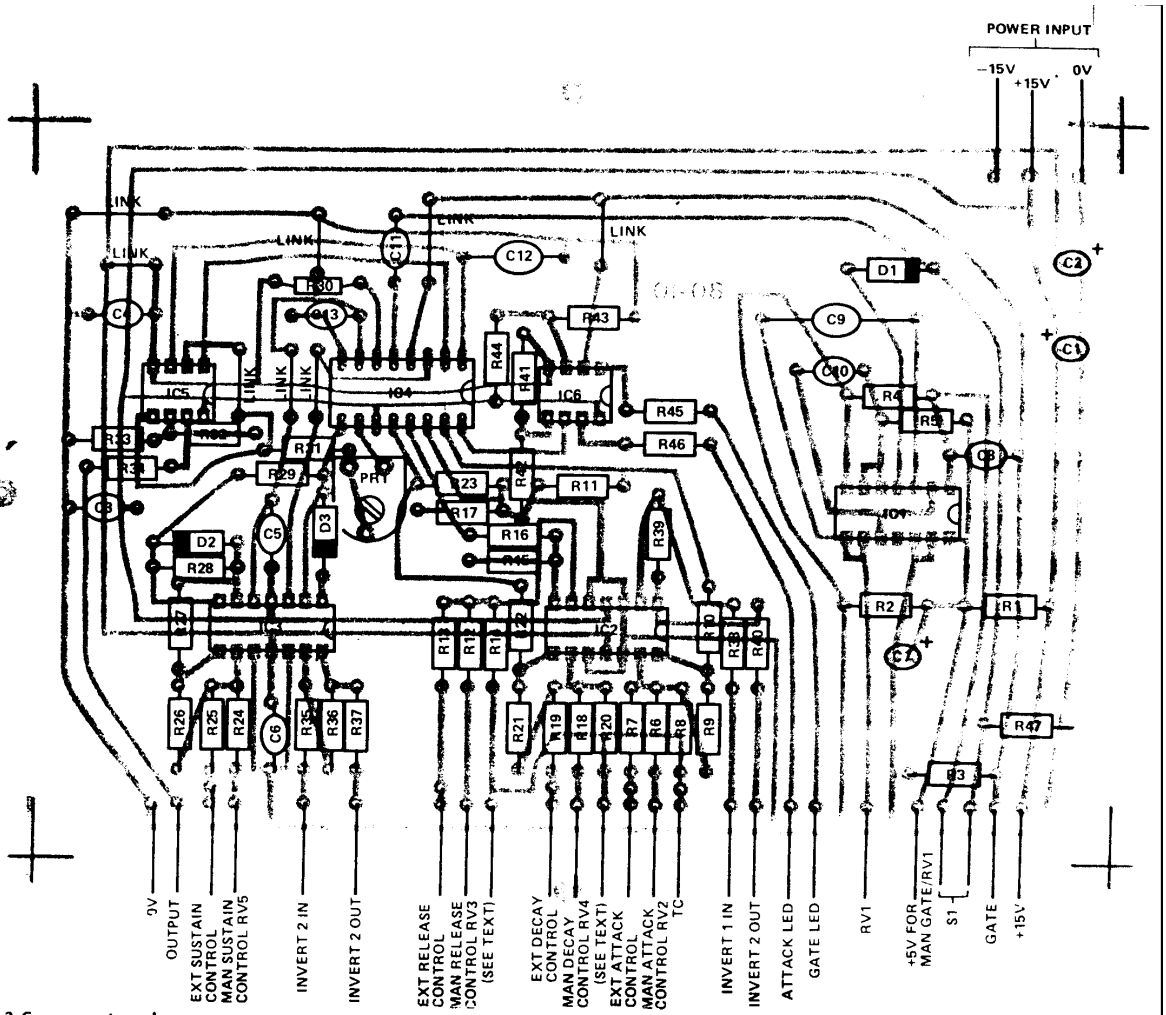


Fig.3. Component overlay

PARTS LIST

Resistors, ¼w, 5% carbon film unless specified.

R1	10k
R2	5k6
R3	47k
R4,6,12,18,24	150k
R5,7,8,13,14,19,20,25,27, 28,32,33,35,36.38,39, 41,44	100k
R9,15,21	62k
R10,16,22	10k 1% metal film
R11,17,23	470R 1% metal film
R26	51k
R29	24k
R30	750R
R31,43	36k
R34,37,40	1k0
R42	1k3
R45,46	1k2
R47	330k

Potentiometers

PR1	10k carbon
RV1	4M7 logarithmic
RV2,3,4,5,6,7	100k linear

Capacitors

C1,2,7	10u 25 V PCB electrolytic
C3,4,5,6	100n polyester
C8	4n7 polycarbonate
C9	1u0 polyester
C10	47n polyester
C11	3n3 polycarbonate
C12	33n polycarbonate
C13	22n polyester

Semiconductors

IC1	4001B
IC2	LM248N
IC3	TL084CP
IC4	CEM3310
IC5	TL082CP
IC6	LM1458N
D1,2,3	1N4148
LED 1	Red LED
LED 2	Green LED

Miscellaneous

SW1	SPST sub-miniature toggle switch
PCB, case, etc.	

sound alters due to the presence of noise and complex waveforms in the transient. A better simulation of this effect is obtained by using two envelope generators, two sound sources, a dual VCA and mixing the outputs from the latter together. In this example the VCES timer is in the delay mode and will initiate an AD envelope when the trigger occurs. It should be noted that only AD envelopes are practical in the delay mode since if the sustain level is above zero the voltage will ramp up to the set level when the gate pulse is received

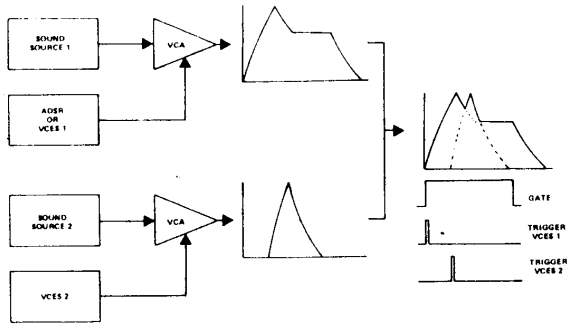


Fig.4. Patch for obtaining realistic transient effects.

Construction

In common with other Project 80 modules the Voltage Controlled Envelope Shaper may be panel mounted or installed in a Teka Alba A23G case. The latter, however, does not have sufficient panel area to neatly accommodate all of the facilities provided. In the cased module illustrated we have omitted the two inverters and controls RV6 and RV7.

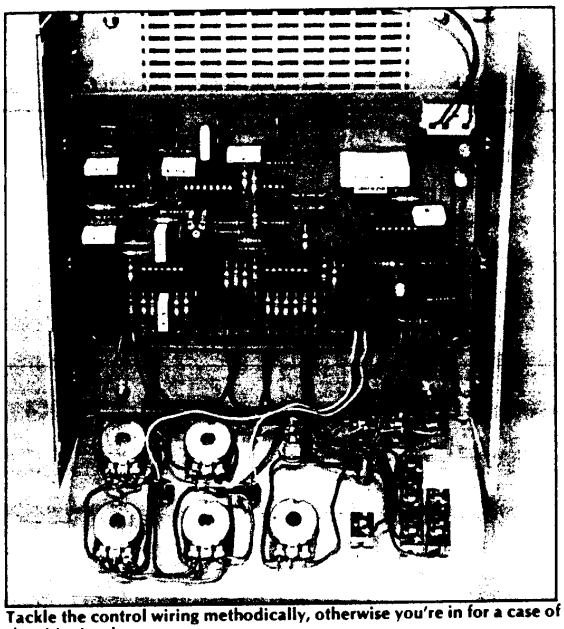
The panel markings for the inverters are − and + and A1 (or A2) with the latter being associated with the attenuating potentiometer RV6 (or RV7). Taking Inverter 1 as the example: R35 is wired to the jack socket marked − at the connection which makes contact with the jack plug; the output of the inverter (R37) is wired to the jack socket marked + but to the connection disabled when a jack plug is inserted, whereas the other connection on this socket is wired to RV6; finally the wiper of RV6 is wired to the make connection on the A1 jack socket. This allows a jack plug into the − socket to access the inverter and the output is obtained at A1, with attenuation when required. For non-inverted voltages which require attenuation these are obtained via the + socket with the output at A1.

One external control of attack, decay and release times is commoned and accessed on the PCB at R8. This allows all three time constants to be altered simultaneously and is connected to jack socket marked TC, denoting time constants. If required, however, the constructor may obtain two independent controls for each time constant by cutting the PCB tracks that join up the inputs of R8, R14 and R20. PCB connections are provided at R14 and R20 to cater for this modification.

The module may be manually gated by connecting a push-to-make switch from the + 5 V line to the gate input.

Calibration and Testing

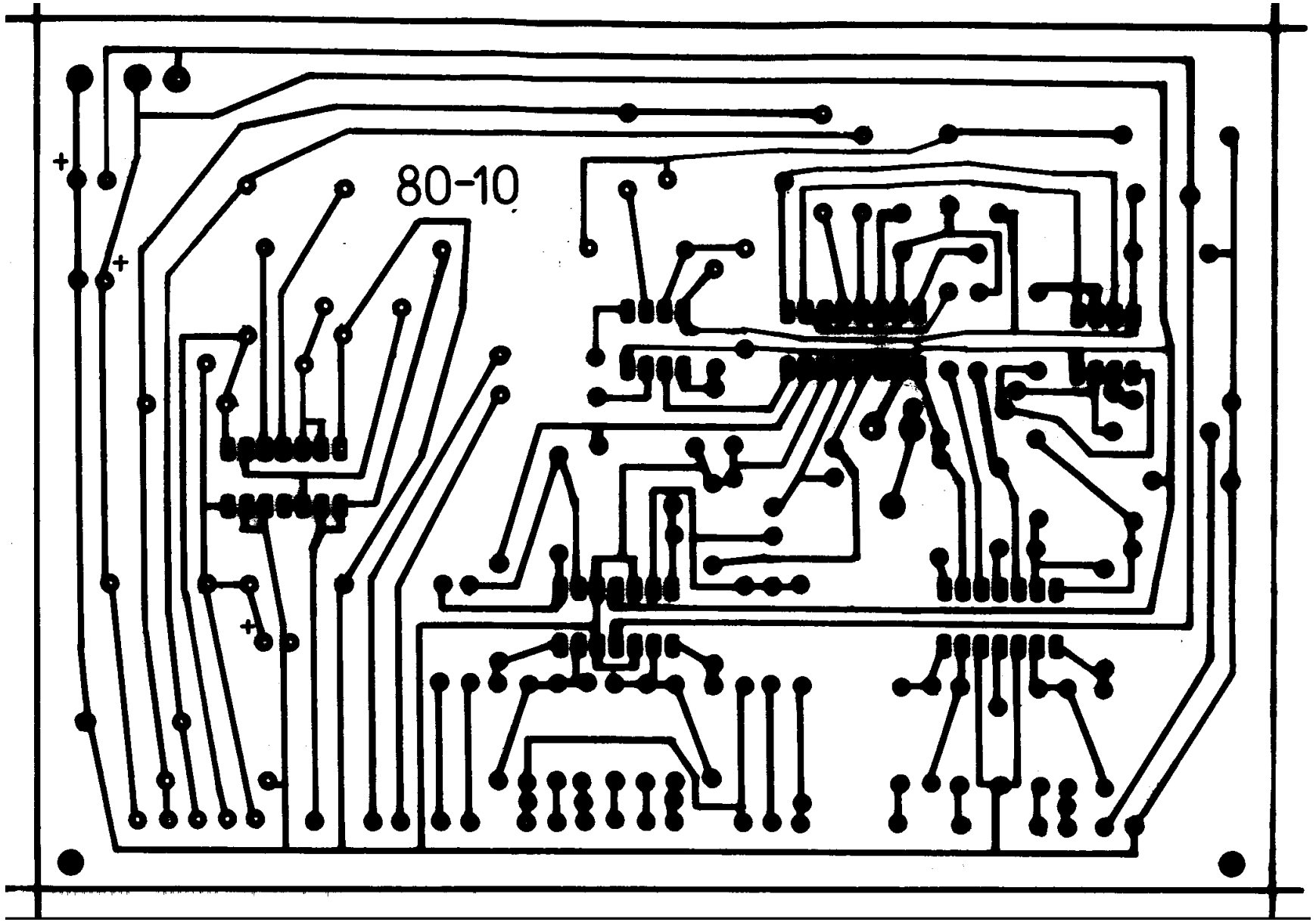
The attack, decay and release manual controls are numbered 0-10 for reference purposes since once external voltages are applied a time calibration becomes meaningless.



Tackle the control wiring methodically, otherwise you're in for a case of the wiring jungles.

PR1 allows more than one module to have the same time constants for a given input voltage. For precise calibration a triggered timing device is required but in most instances the following technique is adequate. Set PR1 to mid-position and connect a voltmeter between ground and the junction of R6 and R9. Turn RV2 until a voltage of −5V6 is obtained. Set all other control pots to zero. Gate the module manually and time the attack time as shown by the attack LED being on. The manual push button is held down until the LED goes off. Gate the unit several times to allow all components to stabilise for this long attack time and then commence adjusting PR1 to give an attack time of 20 S.

Note that the gate LED is only on while the manual button is depressed. Next set the attack time for a short duration, switch to re-trigger mode, turn RV1 fully clockwise and manually gate the module and keep push button held down until the test is complete. The attack LED should come on when the button is first depressed and again about 2.5 S later when the unit re-triggers. Keep settings the same but put the switch into delay mode. In this test the attack LED should come on about 2.5 S after manually gating the unit. Finally connect the output to a VCO which is in turn connected to an audio amplifier and set the attack, decay, sustain and release controls to about mid-position. Gate the module and release the push-button when a steady note is obtained. The test is a simple means of checking that the A,D,S and R functions are all operational. The functioning of the inverters may also be checked in the same way by putting the output from the VCES through the inverters without attenuation prior to the VCO. In this test the envelope will be inverted, that is, the frequency starting high, decreasing, holding steady and then finally going high again.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