| REVISION HISTORY | | | | | |
|---|---|---|---|---|---|
| E.C.N. | ZONE | REV | DESCRIPTION | DATE | APPROVED DWN CHK CM PE |
| | | C | ON SHEET 2: C5 WAS 1000 NOW IS C1 AT 470<br>C189,C289 WERE 330PF R177,R277 WERE 22.1K | 08/03/94 | LCD JM |
| EAT 94-174 | | D | ADD R341,342,343,344,345,346,441,442,443,444,445,446 | 11/07/94 | LCD JM |
| EAT 95-244 | | E | R312,R314,R412,R414 WERE 1W NOW 2W | 09/11/95 | LCD JM |
| EAT 95-217 | | F | CHANGE DISPLAY CONN FROM DIP TO DUAL INLINE<br>DELETE DISPLAY BOARD | 10/09/95 | LCD TS |
| 00N0006 | | G | CHANGE Q100,126,200,226 TO C 7458-0. CHANGE U100,200 TO 103309-1. CHANGE U103,203 TO 103308-1. | 02/04/00 | JAW JG KZ KB |

BALANCED TO UNBALANCED INPUT STAGE

GAIN STAGE
VOLUME CONTROL/FRONT PANEL

LAST VOLTAGE AMP

OUTPUT BOARD

HIGH-SIDE NPN DRIVER AND OUTPUT

LOW-SIDE NPN DRIVER AND OUTPUT

REAR PANEL OUTPUT

PRE-DRIVER

LOW-SIDE ERROR AMP

BIAS STRING

HIGH-SIDE ERROR AMP

VOLTAGE TRANSLATOR STAGE

ODEP

PRE-DRIVER

HIGH-SIDE PNP DRIVER AND OUTPUT

LOW-SIDE PNP DRIVER AND OUTPUT

FAULT CIRCUIT

BUFFER

TURN ON DELAY AND FAULT OUTPUT

DC/LF PROTECT

STEREO-MONO SWITCH (S4)

PARALLEL
STEREO
BRIDGE

**INACTIVE**
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DISTRIBUTION: G

TOLERANCE UNLESS OTHERWISE SPECIFIED
.00 = ±.02"
.000 = ±.010"
DRILLS = ±.003"

DO NOT SCALE DRAWING

| | | |
|---|---|---|
| DWN | LCD | 12/08/93 |
| CHK | | |
| CM | | |
| PE | JM | 12-22-93 |


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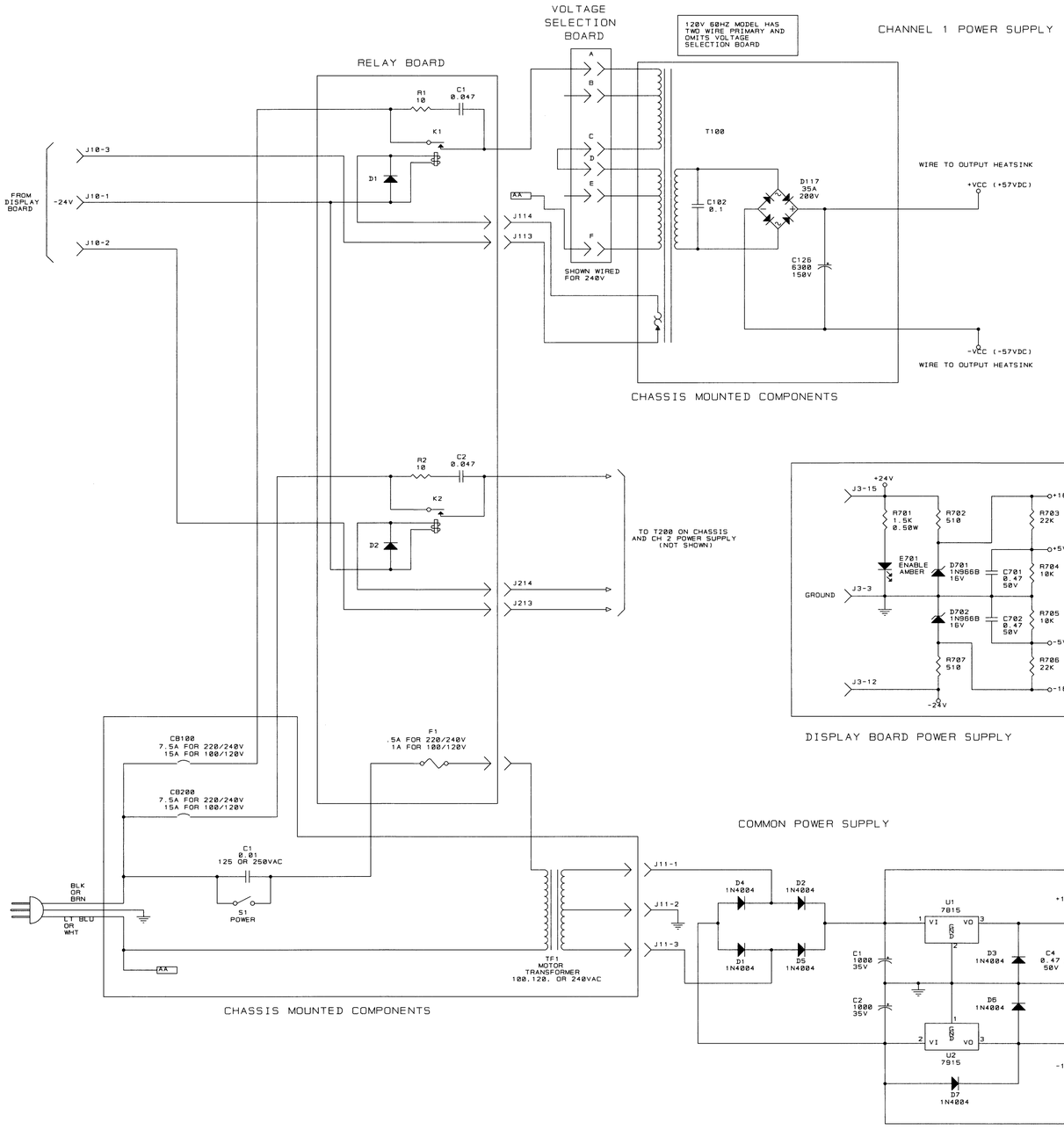
TITLE: SCH, MA-2400/MA-2401

SIZE D | DWG NO. J0625-4 | REV G

SCALE NONE | PROJ NO. MD26450 | SHEET 1 OF 3




## COMMON

| LAST USED | OBSOLETED |
|---|---|
| C7 | |
| D7 | |
| R10 | R5,6,11-15 |
| S4 | |
| U2 | |

## CHANNEL 1

| LAST USED | OBSOLETED |
|---|---|
| C157 | C121,131,132,142 |
| D132 | D100-103,116,118,119 |
| N102 | N100 |
| Q124 | Q104,111,114 |
| R199 | R100,169,172,178 |
| R921 | R900-905 |
| U104 | |

NOTES :

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
3. CHANNEL 1 SHOWN. FOR CHANNEL 2 ADD 100 TO REFERENCE DESIGNATORS. (EXAMPLE : CHANNEL 1 R101 WOULD BE CHANNEL 2 R201.) CONNECTOR AND IC PIN NUMBERS FOR CHANNEL 2 ARE SHOWN IN PARENTHESIS WHEN THEY DIFFER FROM CHANNEL 1.
4. ALL DIODES ARE 1N4148 UNLESS OTHERWISE SPECIFIED.
5. ON J500 AND J700 THE STRIPED WIRE GOES TO PIN 10 OF THE BOARD AND THE PIN NUMBERS MOLDED ON THE CABLE SOCKET ARE REVERSED FROM THE PIN NUMBERS ON THE BOARD AND THE SCHEMATIC.
6. STANDARD UNIT HAS R10 OPEN. INSTALL JUMPER IN R10 TO DISABLE CHANNEL 2 SIGNAL/IOC LIGHT IN PARALLEL MONO MODE.
7. POWER SUPPLY VOLTAGES SHOWN UNDER NO LOAD CONDITION.
8. CHANNEL 2 PRE-DRIVER BASES LOOP THROUGH STEREO-MONO SWITCH S4, SECTIONS E AND F.
9. THIS SCHEMATIC REVISION APPLIES TO MAIN BOARD D8369-7 / MODULE Q43257-7 AND OUTPUT BOARD P10433-4 / MODULE Q43358-3.

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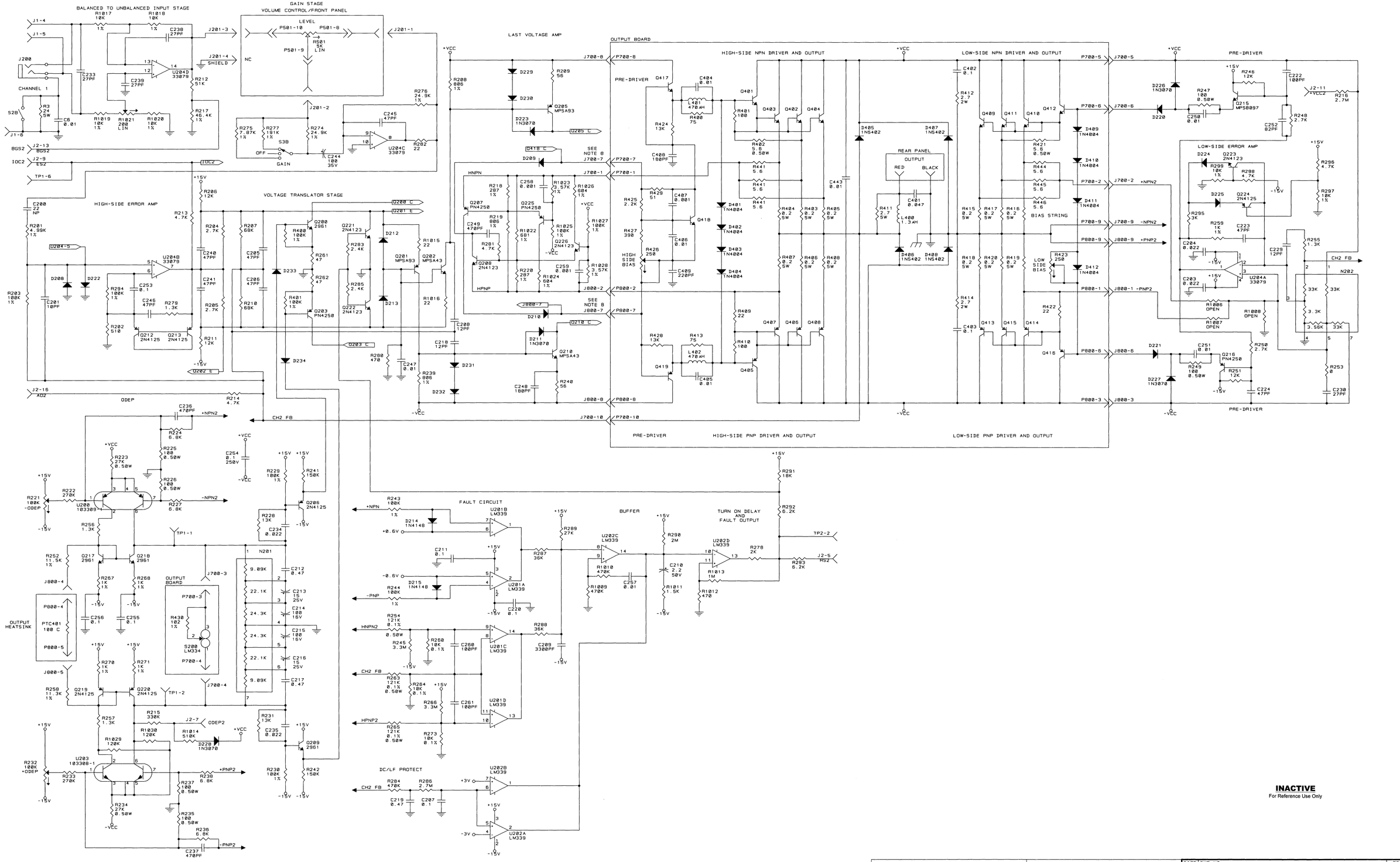
| SIZE | DWG NO. | REV |
|---|---|---|
| D | J0625-4 | G |
| SCALE NONE | PROJ NO. MD26450 | SHEET 2 OF 3 |

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| SIZE | DWG NO. | REV |
|---|---|---|
| D | J0625-4 | G |
| SCALE NONE | PROJ NO. MD26450 | SHEET 3 OF 3 |