AKAI

MODEL S5000
MODEL S6000

SCHEMATIC DIAGRAMS AND PC BOARDS

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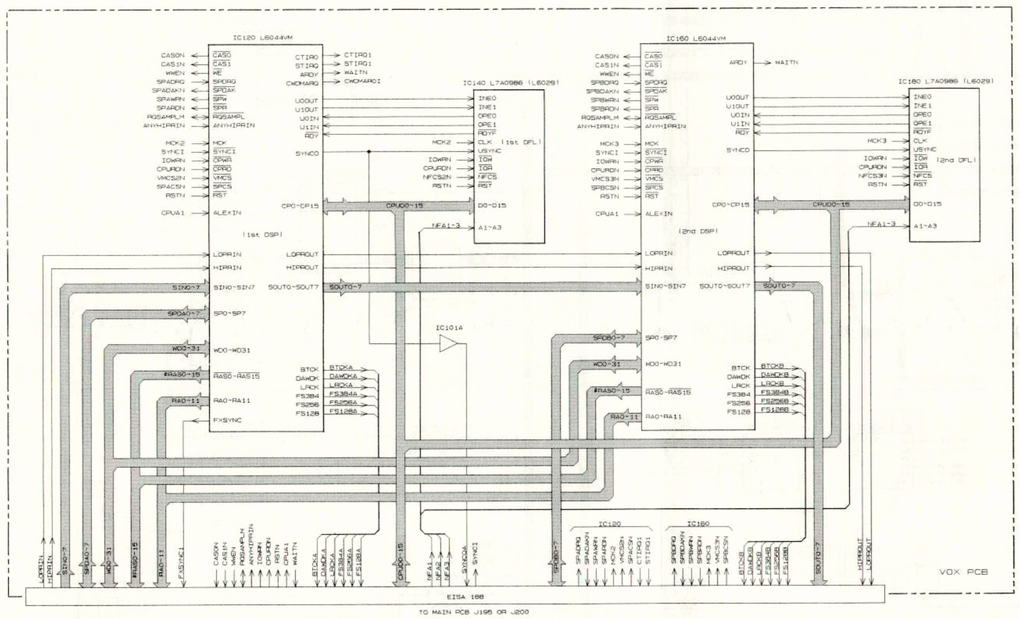
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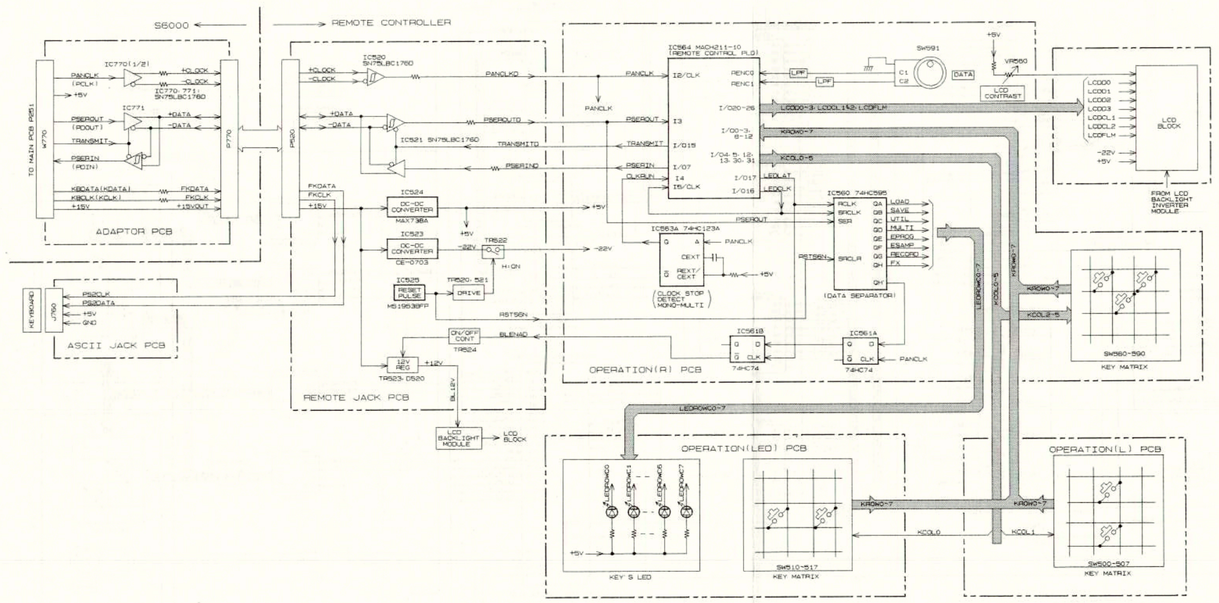
III. INFORMATION OF ICs 33

Use these schematic diagrams and PC boards together with the provided service manual.

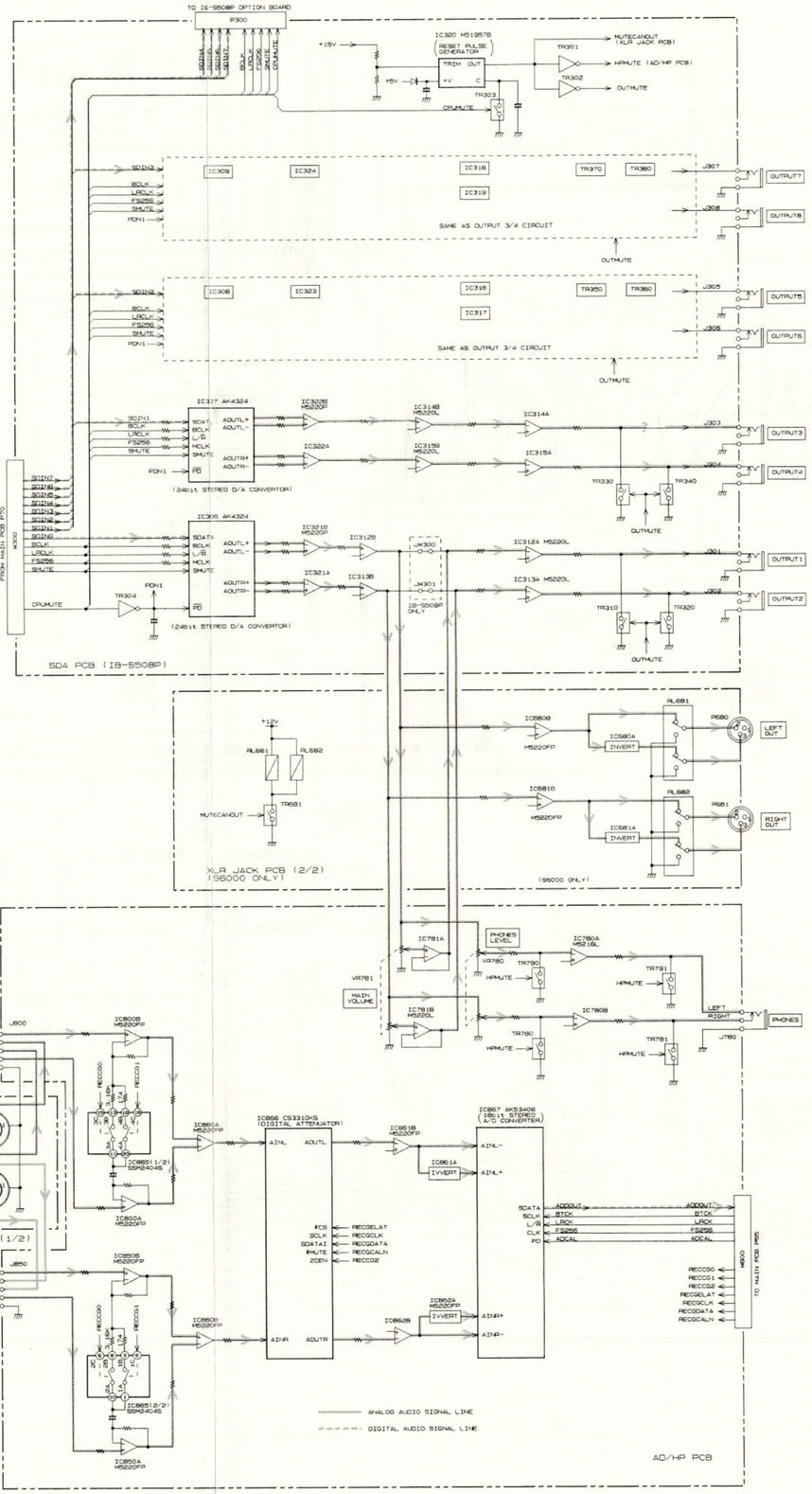
TO VDK54 (VOICE EXPANSION) PCB
TO 2nd VDK54 (VOICE EXPANSION) PCB (OPTION)
SIMM x 4
FOR OPTION BOARD
TO IB-1616A DIGITAL AUDIO EXPANSION BOARD
TO EMIO EFFECT BOARD (OPTION)
TO AD/HP PCB W800
TO SDA PCB W300
TO INTERNAL IDE DEVICE (OPTION)
SCSI PCB
MIDI (A) PCB
MIDI (B) PCB
MAIN PCB
ASCII JACK PCB
OPERATION(L) PCB
OPERATION (R) PCB
KEYMATRIX
KEYBOARD
LCD BLOCK
S5000 ONLY
TO ADAPTOR PCB (S6000 ONLY)
S5000/6000
MAIN
BLOCK DIAGRAM
NO.2-1 L6044851M



VOX64
BLOCK DIAGRAM

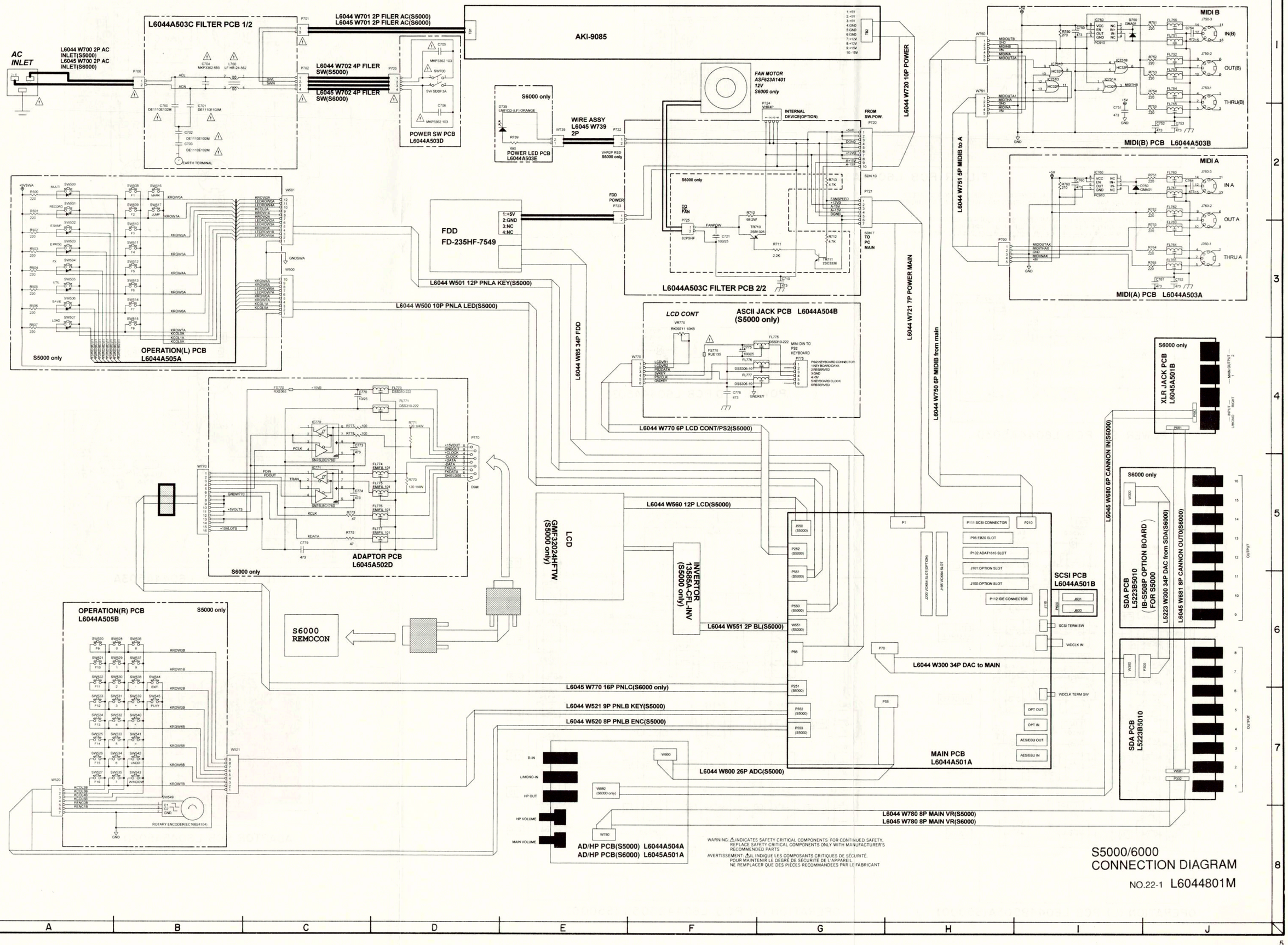


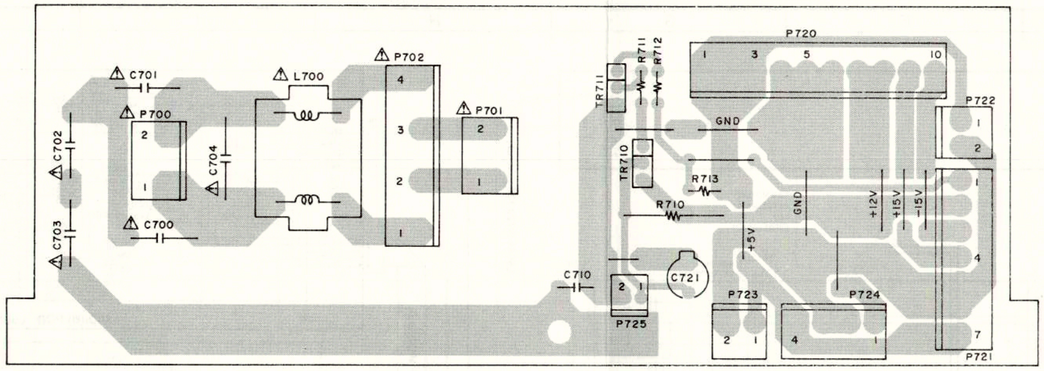
S6000 REMOTE CONTROL
BLOCK DIAGRAM



A/D & D/A
BLOCK DIAGRAM

S5000/6000
PERIPHERAL CIRCUIT
BLOCK DIAGRAM
NO.2-2 L6044852M

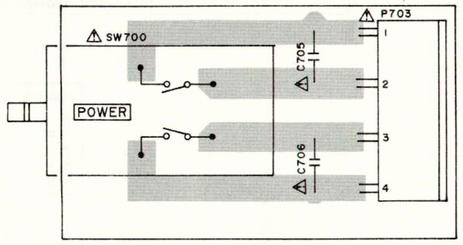

AC INLET
L6044 W700 2P AC INLET(S5000)
L6045 W700 2P AC INLET(S6000)
L6044A503C FILTER PCB 1/2
L6044 W701 2P FILER AC(S5000)
L6045 W701 2P FILER AC(S6000)
L6044 W702 4P FILER SW(S5000)
L6045 W702 4P FILER SW(S6000)
POWER SW PCB L6044A503D
AKI-9085
L6044 W720 10P POWER
FAN MOTOR ASF623A1401 12V S6000 only
S6000 only
POWER LED PCB L6044A503E
WIRE ASSY L6045 W739 2P
INTERNAL DEVICE(OPTION)
FROM SW.POW. P720
L6044A503C FILTER PCB 2/2
FDD FD-235HF-7549
L6044 W501 12P PNLA KEY(S5000)
L6044 W500 10P PNLA LED(S5000)
OPERATION(L) PCB L6044A505A
S5000 only
L6044 W721 7P POWER MAIN
L6044 W750 9P MIDIB from main
MIDI B
MIDI(B) PCB L6044A503B
L6044 W751 5P MIDIB to A
MIDI A
MIDI(A) PCB L6044A503A
LCD CONT
ASCII JACK PCB L6044A504B (S5000 only)
L6044 W770 6P LCD CONT/PS2(S5000)
L6044 W65 34P FDD
ADAPTOR PCB L6045A502D
L6044 W560 12P LCD(S5000)
LCD GMF32024HFTW (S5000 only)
INVERTER 13585A-CFL-INV (S5000 only)
L6044 W551 2P BL(S5000)
S6000 REMOCON
SCSI PCB L6044A501B
L6044 W300 34P DAC to MAIN
L6045 W770 16P PNLC(S6000 only)
L6044 W521 9P PNLB KEY(S5000)
L6044 W520 8P PNLB ENC(S5000)
MAIN PCB L6044A501A
L6044 W800 26P ADC(S5000)
L6044 W780 8P MAIN VR(S5000)
L6045 W780 8P MAIN VR(S6000)
L6045 W680 8P CANNON IN(S6000)
XLR JACK PCB L6045A501B
SDA PCB L5223B5010 (IB-S508P OPTION BOARD) FOR S5000
L5223 W300 34P DAC from SDA(S6000)
L6045 W681 8P CANNON OUT(S6000)
SDA PCB L5223B5010
AD/HP PCB(S5000) L6044A504A
AD/HP PCB(S6000) L6045A501A
OPERATION(R) PCB L6044A505B
WARNING: ⚠ INDICATES SAFETY CRITICAL COMPONENTS. FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS.
AVERTISSEMENT: ⚠ IL INDIQUE LES COMPOSANTS CRITIQUES DE SÉCURITÉ. POUR MAINTENIR LE DEGRÉ DE SÉCURITÉ DE L'APPAREIL, NE REMPLACER QUE DES PIÈCES RECOMMANDÉES PAR LE FABRICANT
S5000/6000 CONNECTION DIAGRAM
NO.22-1 L6044801M



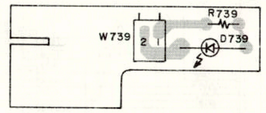
FILTER PCB L6044A503C

WARNING: ⚠ INDICATES SAFETY CRITICAL COMPONENTS. FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS

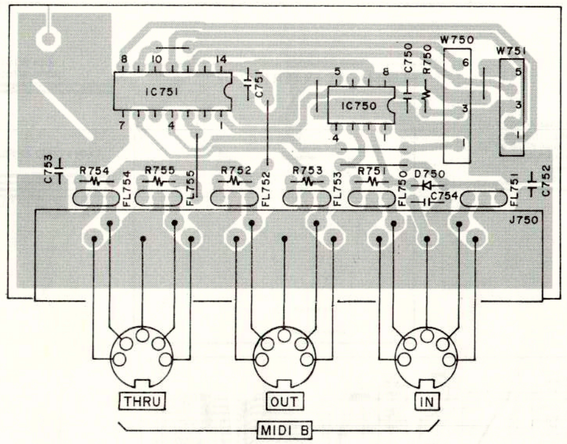
AVERTISSEMENT: ⚠ IL INDIQUE LES COMPOSANTS CRITIQUES DE SÉCURITÉ. POUR MAINTENIR LE DEGRÉ DE SÉCURITÉ DE L'APPAREIL, NE REMPLACER QUE DES PIÈCES RECOMMANDÉES PAR LE FABRICANT



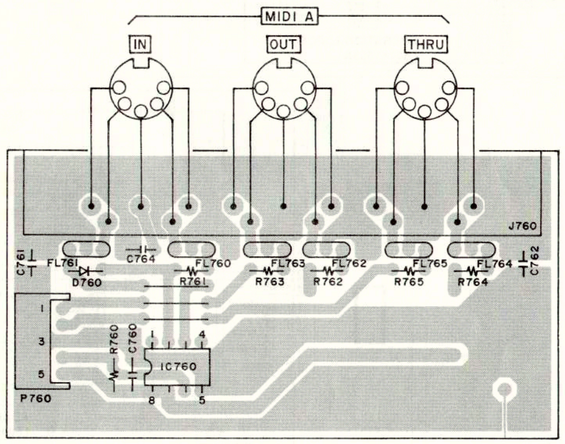
POWER SW PCB L6044A503D



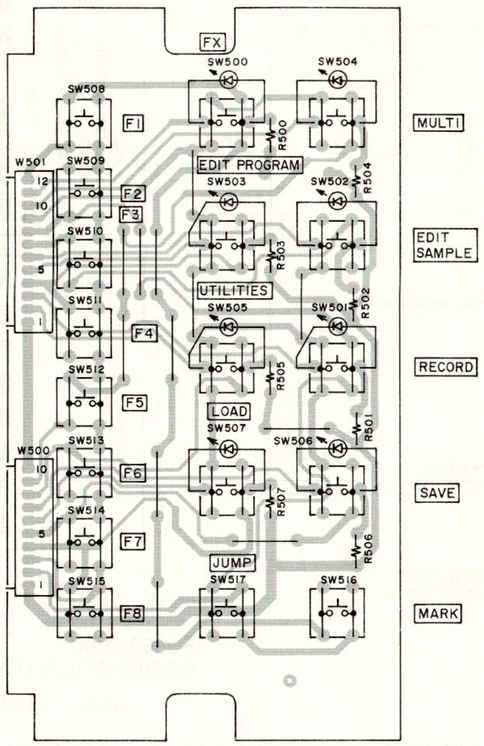
POWER LED PCB L6044A503E



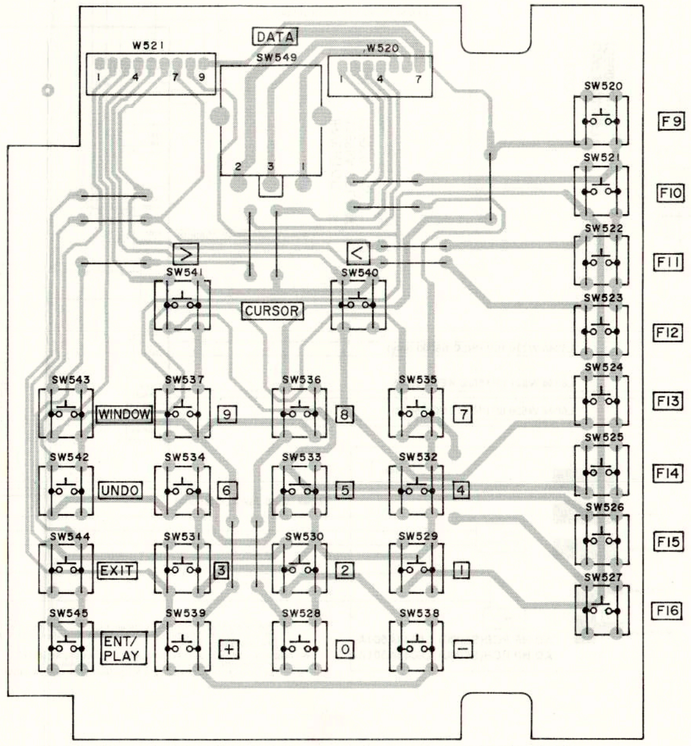
MIDI (B) PCB L6044A503B



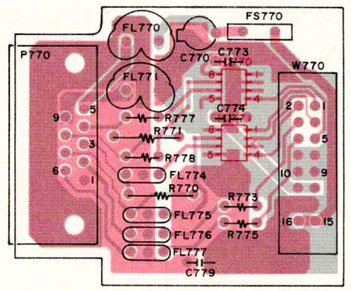
MIDI (A) PCB L6044A503A



OPERATION (L) PCB L6044B505A(S5000)



OPERATION (R) PCB L6044B505B (S5000)



ADAPTOR PCB L6045A502D (S6000)

CPU D-RAM ROM F-ROM

CPU

FDC and RTC

(2/11)

(3/11)

PANEL CONT

(4/11)

S6000 only
FL16
DSS306-222

POWER INPUT

TO FILTER PCB P721

to dc-dc conv

to I/O slot

to adc/dac

A/D CONVERTER SOCKET

TO AD / HP PCB W800

LRCLK SELECTOR,CLOCK GENERATOR AND PHASE LOCK DETECTION

(5/11)

(1/11)

(6/11)

DIO

(7/11)

SCSI CONTROLLER

(8/11)

I/O SOCKETS

(9/11)

VOICE SOCKET

(10/11)

VOICE EXPANSION SOCKET

WAVE RAM

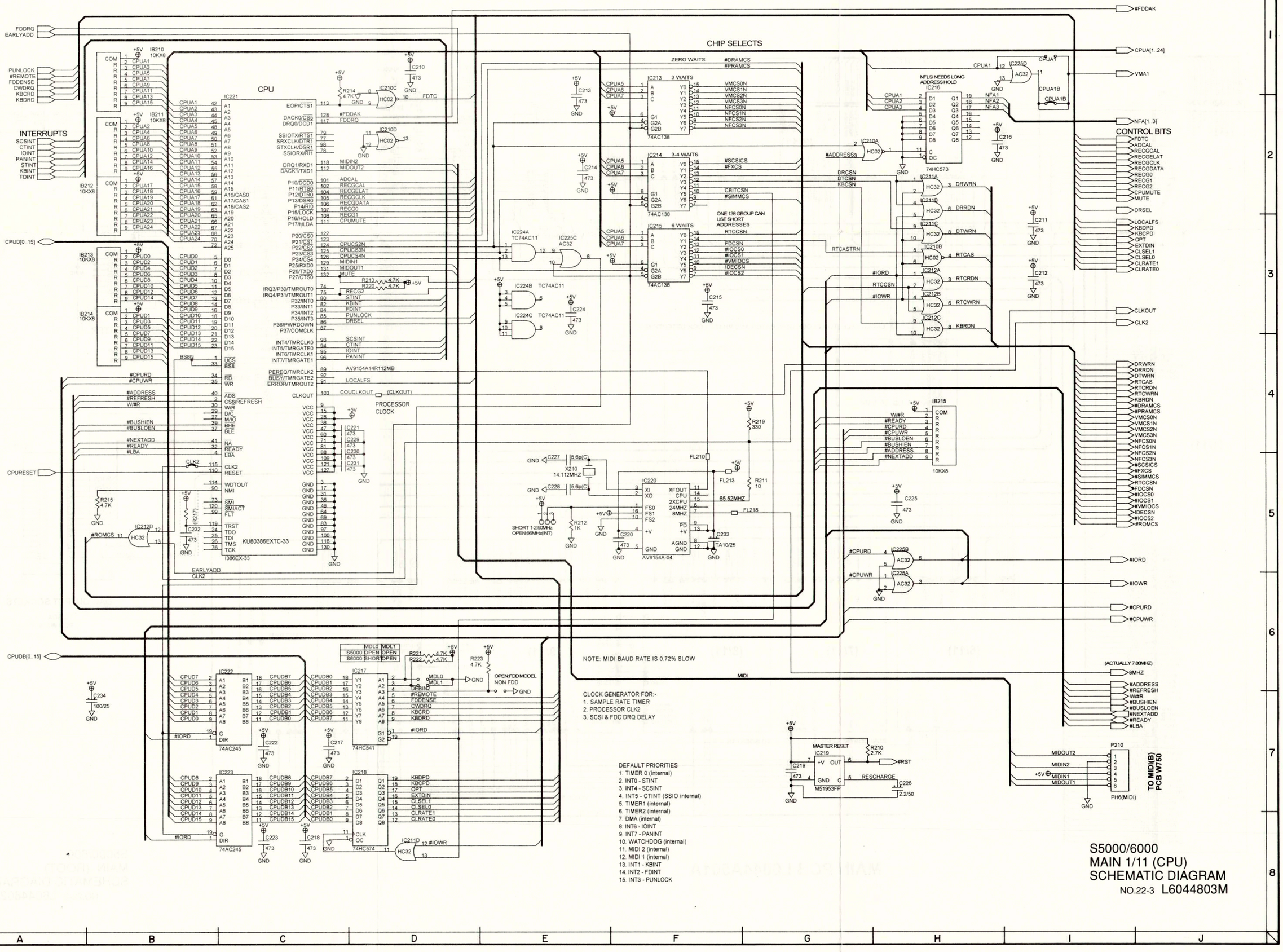
(11/11)

DAC OUTPUT SOCKETS

TO SDA PCB W300

MAIN PCB L6044A501A

S5000/6000
MAIN (ROOT)
SCHEMATIC DIAGRAM
NO.22-2 L6044802M


CHIP SELECTS
CPU
INTERRUPTS
PROCESSOR CLOCK
CONTROL BITS
ZERO WAITS
3 WAITS
3-4 WAITS
6 WAITS
ONE 138 GROUP CAN USE SHORT ADDRESSES
NFLSI NEEDS LONG ADDRESS HOLD
KU80386EXTC-33
I386EX-33
AV9154A-04
74AC138
74HC573
74AC245
74HC541
74HC574
M51953FP
NOTE: MIDI BAUD RATE IS 0.72% SLOW
MIDI
CLOCK GENERATOR FOR:-
1. SAMPLE RATE TIMER
2. PROCESSOR CLK2
3. SCSI & FDC DRQ DELAY
DEFAULT PRIORITIES
1. TIMER 0 (internal)
2. INT0 - STINT
3. INT4 - SCSINT
4. INT5 - CTINT (SSIO internal)
5. TIMER1 (internal)
6. TIMER2 (internal)
7. DMA (internal)
8. INT6 - IOINT
9. INT7 - PANINT
10. WATCHDOG (internal)
11. MIDI 2 (internal)
12. MIDI 1 (internal)
13. INT1 - KBINT
14. INT2 - FDINT
15. INT3 - PUNLOCK
TO MIDI(B) PCB W750
S5000/6000
MAIN 1/11 (CPU)
SCHEMATIC DIAGRAM
NO.22-3 L6044803M

NOTE: 72068 DATA STATES THAT 32MHZ CLOCK MUST BE WITHIN +/- 0.5%

C89 10p(C) FDCX1
X85 32MHz
R85 2.2K
C90 10p(C) FDCX2
GND

IC86 UPD72068GF

XA1 48
XA2 49
XB1 51
XB2 52

RESET 18
INT 38
CS 21
RD 19
WR 20
A0 22

FDCSN
#CPURD
#IOWR
CPUA1

CPUD0 25 D0
CPUD1 26 D1
CPUD2 27 D2
CPUD3 28 D3
CPUD4 30 D4
CPUD5 31 D5
CPUD6 32 D6
CPUD7 34 D7

IC85 74HC164
1uS delay of rising edge of DMARQ
(ACTUALLY 7.88 MHZ)
+5V

8MHZ
#FDDAK
FDTC

DMARQ 35
DMAAK 36
TC 37

VDD1 11
VDD1 12
C86 10/25
C87 473

GND1 24
GND1 29
GND1 33
GND1 47
GND1 50
GND1 53

GND2 5
GND2 8
GND2 55
GND2 58
GND2 61
GND2 64
GND2 68
GND2 72
GND2 75

C85 473

MSEL 17
ENRW 15
RSEL 16
FMT 39
DR0 40
DR1 41
PCS0 45
PCS1 46
ACTL 14
FLT 3
FLTR 6
LCT 10
ENPCS 13
HDLD 7
DEN0 54
DEN1 56
2SIDE 1
INDEX 44
DS0 62
DS1 60
DS2 59
DS3 57
EM0 69
EM1 67
EM2 66
EM3 63
DIR 70
STEP 73
WDATA 74
WE 76
TRK0 77
WRPT 78
RDATA 79
SIDE 4
READY 80

NC 2
NC 9
NC 23
NC 42
NC 43
NC 65
NC 71

DISKCHN
INDEXN
DSEL0N
MOTORONN
DIRN
STEPN
WDATAN
WGATEN
TRK0N
WPROTN
RDATAN
SIDE1N
FDDRDYN

FDDENSE

IB85 10KX8
COM
R

P85 FAN34(FDD)
HIDEN
DSEL3
INDEX
DSEL0
DSEL1
DSEL2
MOTON
DIR
STEP
WDATA
WGATE
TRK0
WPROT
RDATA
SIDE1
RDY/CH
GND

TO FDD UNIT

DISK CHANGE(DEFAULT)
CUT and SHORT:READY

FLOPPY DISK CONTROLLER

FDINT
FDDRQ

CPUDB[0..7]

IC5 RTC-6593
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AS
CS
RD-DS
R/W
IRQ
RESET
X1
X2
MOT
SQW
NC
RCLR
+5V
VBAT
GND

INTEL CPU MODE

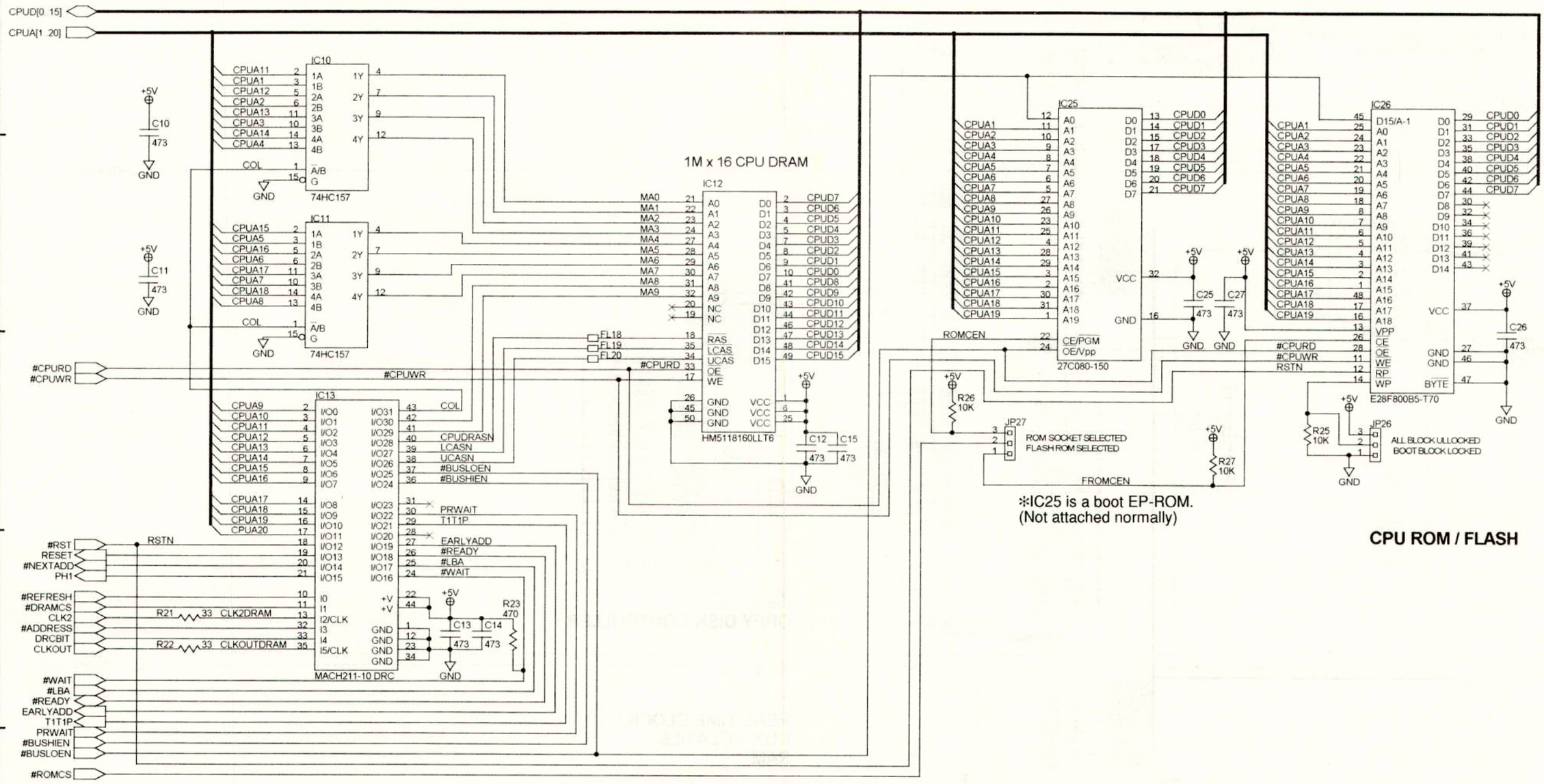
RTCAS
RTCCSN
RTCRDN
RTCWRN
#RST

D5 1S30E
R5 5.1K
Battery in Socket
J5 BH25T
C5 473
C6 473

Power-down drain approx 0.5uA @ 25C

REAL-TIME CLOCK / NON-VOLATILE RAM

S5000/6000
MAIN 2/11
(FDC and REAL-TIME CLOCK)
SCHEMATIC DIAGRAM
NO.22-4 L6044804M



*IC25 is a boot EP-ROM.
(Not attached normally)

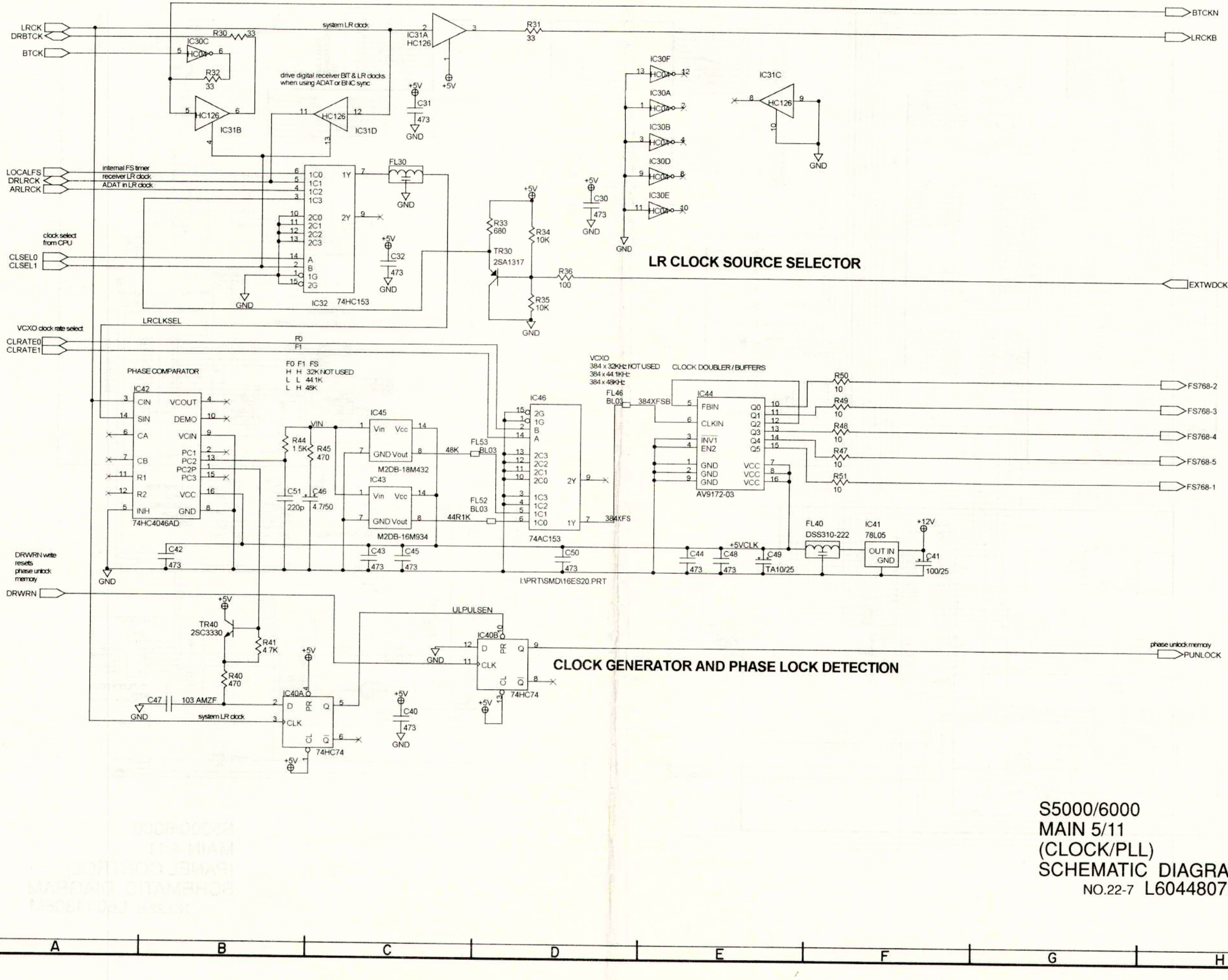
CPU ROM / FLASH

CPU DRAM & CONTROLLER

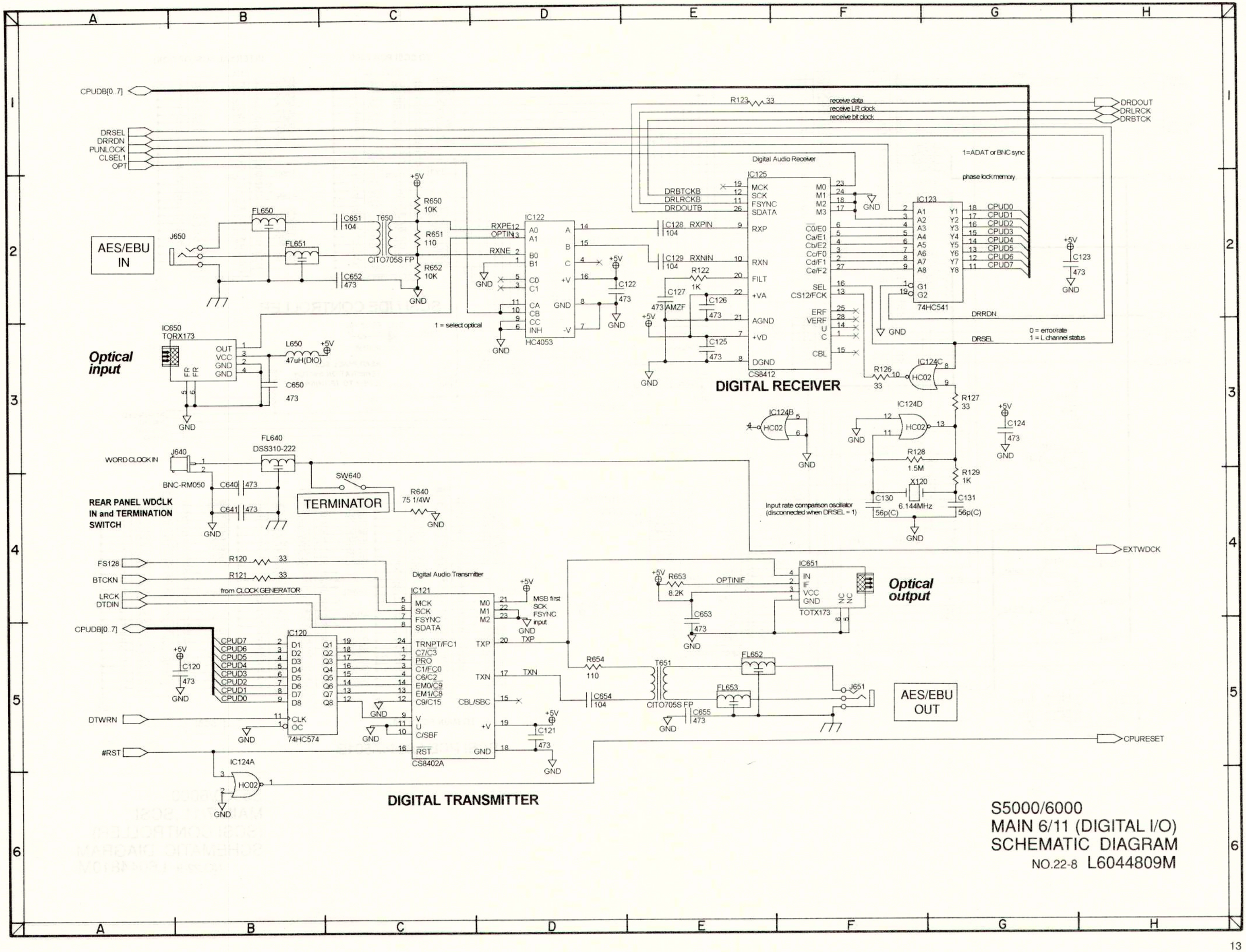
S5000/6000
MAIN 3/11
(CPU D-RAM/ROM/F-ROM)
SCHEMATIC DIAGRAM
NO.22-5 L6044805M

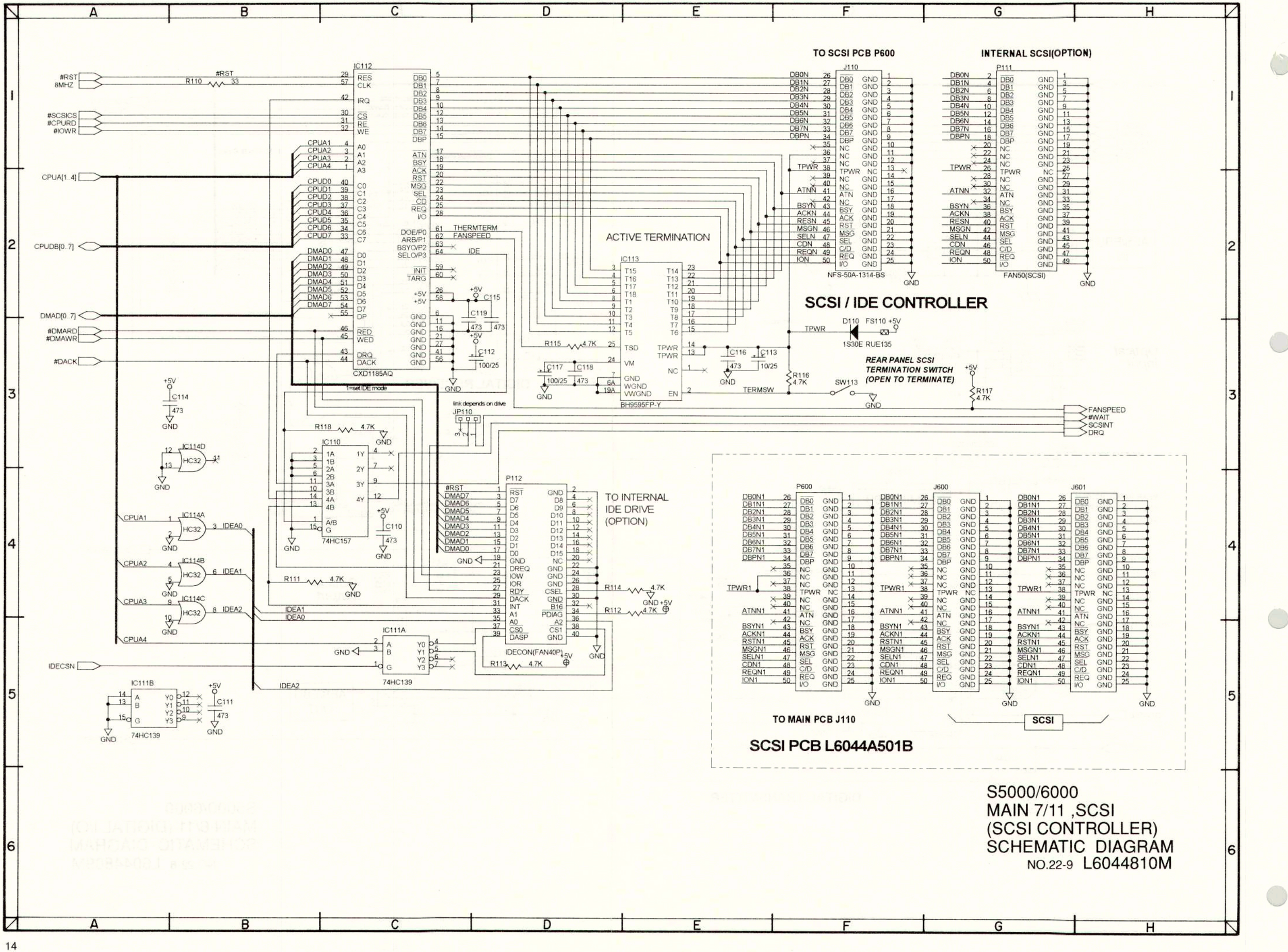
S5000/6000
MAIN 4/11
(PANEL CONTROL)
SCHEMATIC DIAGRAM

NO.22-6 L6044806M

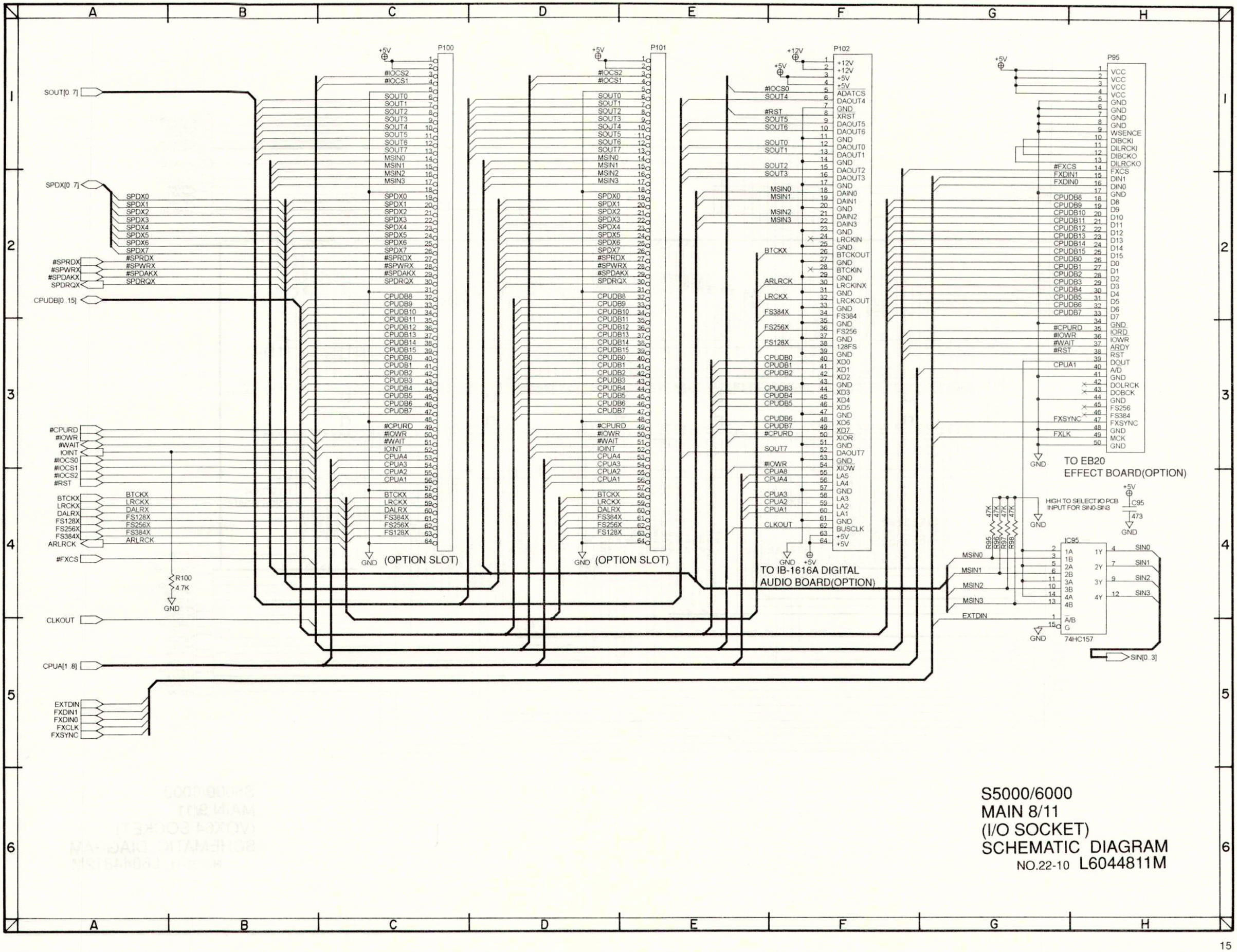


S5000/6000
MAIN 5/11
(CLOCK/PLL)
SCHEMATIC DIAGRAM
NO.22-7 L6044807M

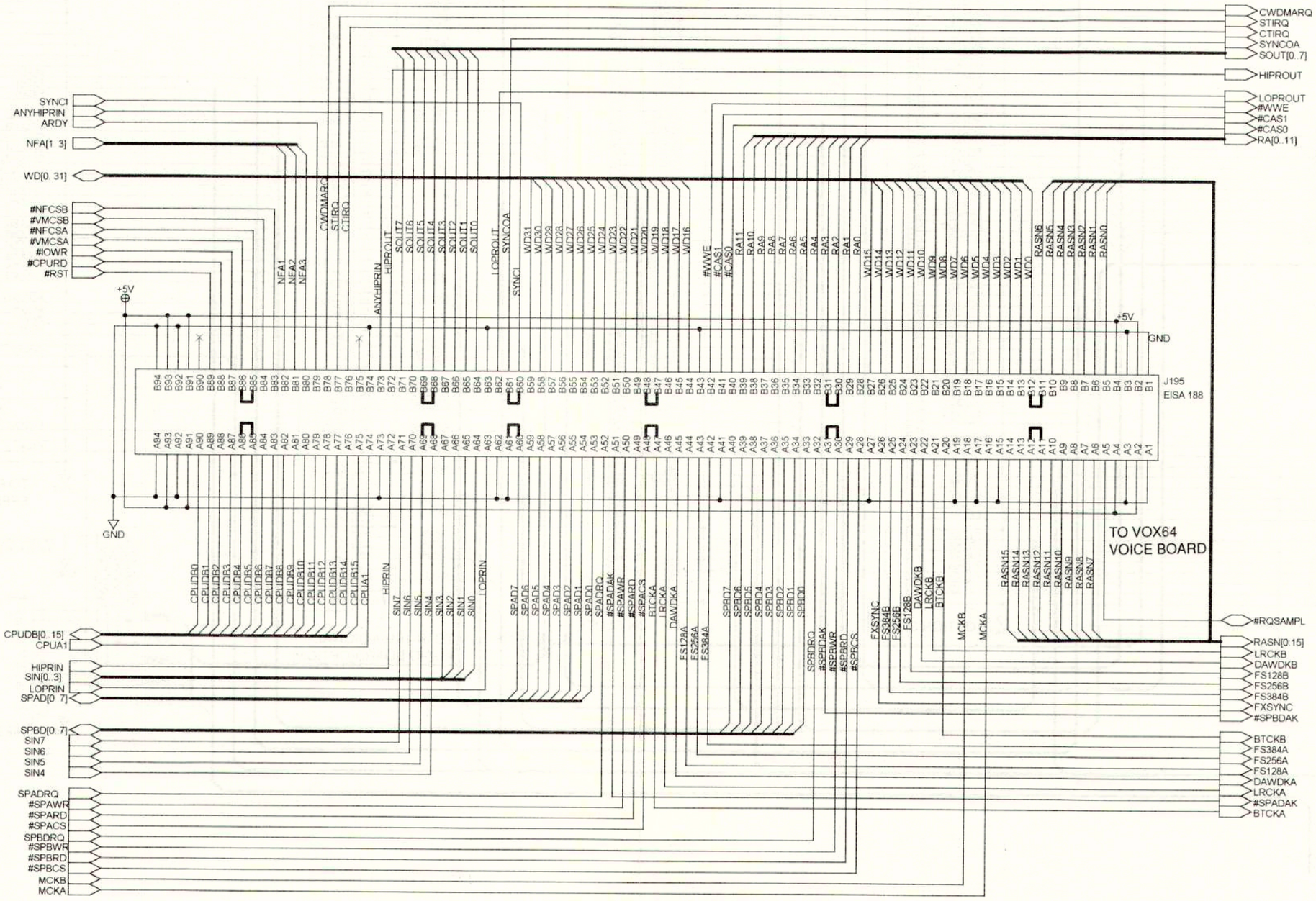

CPUDB[0..7]
DRSEL
DRRDN
PUNLOCK
CLSEL1
OPT
R123 33
receive data
receive LR clock
receive bit clock
DRDOUT
DRLRCK
DRBTCK
1=ADAT or BNC sync
phase lock memory
Digital Audio Receiver
IC125
DRBTCKB
DRLRCKB
DRDOUTB
MCK
SCK
FSYNC
SDATA
RXP
RXN
FILT
+VA
AGND
+VD
DGND
CS8412
M0
M1
M2
M3
C0/E0
Ca/E1
Cb/E2
Cc/F0
Cd/F1
Ce/F2
SEL
CS12/FCK
ERF
VERF
U
C
CBL
IC123
74HC541
DRRDN
CPUD0
CPUD1
CPUD2
CPUD3
CPUD4
CPUD5
CPUD6
CPUD7
C123 473
0 = error/rate
1 = L channel status
DRSEL
AES/EBU IN
J650
FL650
FL651
C651 104
C652 473
T650
CITO705S FP
R650 10K
R651 110
R652 10K
IC122
HC4053
RXPE
OPTIN
RXNE
1 = select optical
C128 RXPIN 104
C129 RXNIN 104
R122 1K
C127 473 AMZF
C126 473
C125 473
C122 473
Optical input
IC650
TORX173
L650 47uH(DIO)
C650 473
DIGITAL RECEIVER
IC124C HC02
R126 33
R127 33
IC124B HC02
IC124D HC02
R128 1.5M
R129 1K
X120 6.144MHz
C130 56p(C)
C131 56p(C)
C124 473
Input rate comparison oscillator (disconnected when DRSEL = 1)
WORD CLOCK IN
J640
FL640
DSS310-222
BNC-RM050
C640 473
C641 473
SW640
TERMINATOR
R640 75 1/4W
REAR PANEL WDCLK IN and TERMINATION SWITCH
EXTWDCK
FS128
BTCKN
LRCK
DTDIN
from CLOCK GENERATOR
R120 33
R121 33
Digital Audio Transmitter
IC121
CS8402A
MSB first
SCK
FSYNC input
TXP
TXN
IC120
74HC574
DTWRN
#RST
IC124A HC02
DIGITAL TRANSMITTER
IC651
TOTX173
R653 8.2K
OPTINIF
C653 473
Optical output
R654 110
T651
CITO705S FP
FL652
FL653
C654 104
C655 473
J651
AES/EBU OUT
CPURESET
S5000/6000
MAIN 6/11 (DIGITAL I/O)
SCHEMATIC DIAGRAM
NO.22-8 L6044809M



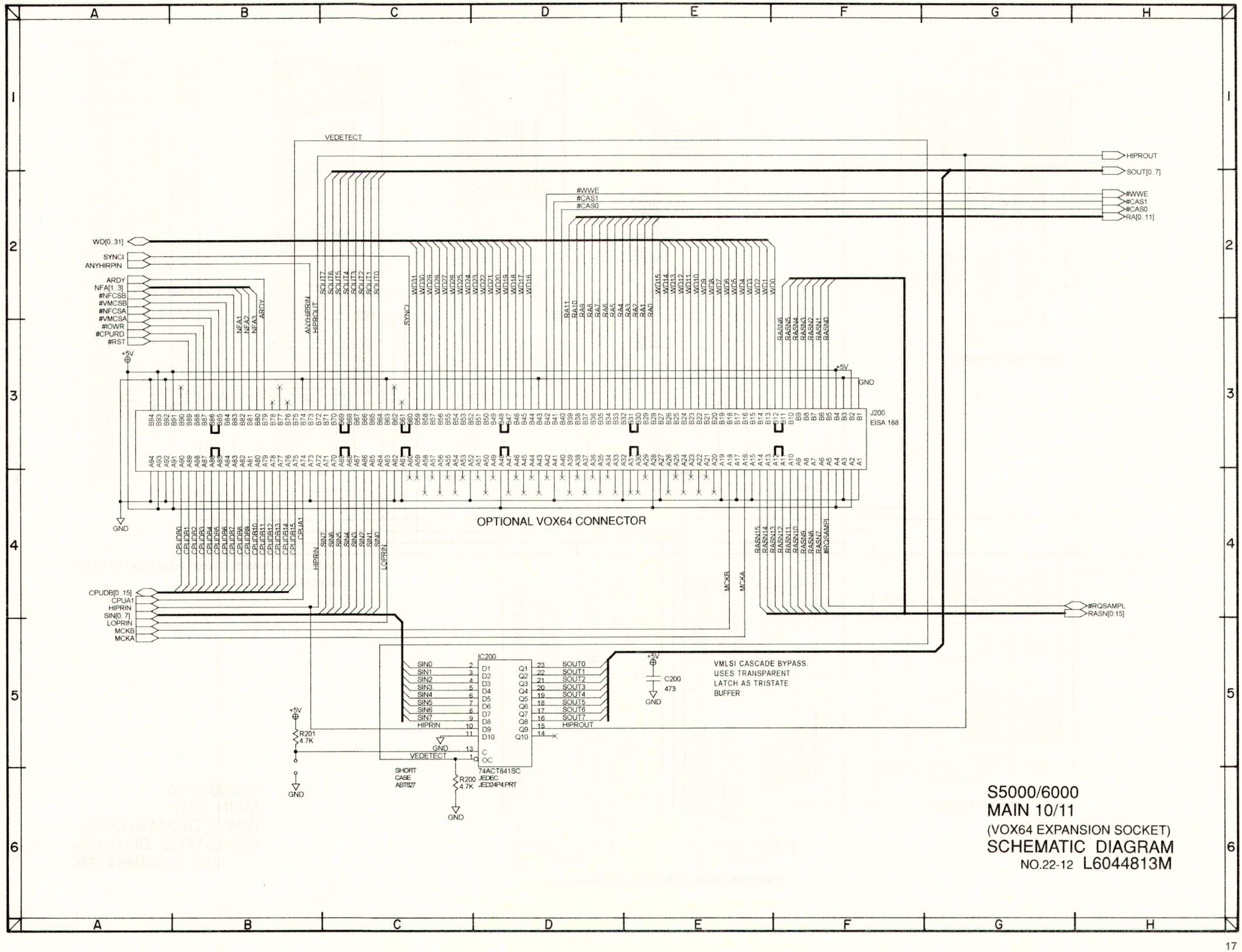
S5000/6000
MAIN 7/11 ,SCSI
(SCSI CONTROLLER)
SCHEMATIC DIAGRAM
NO.22-9 L6044810M



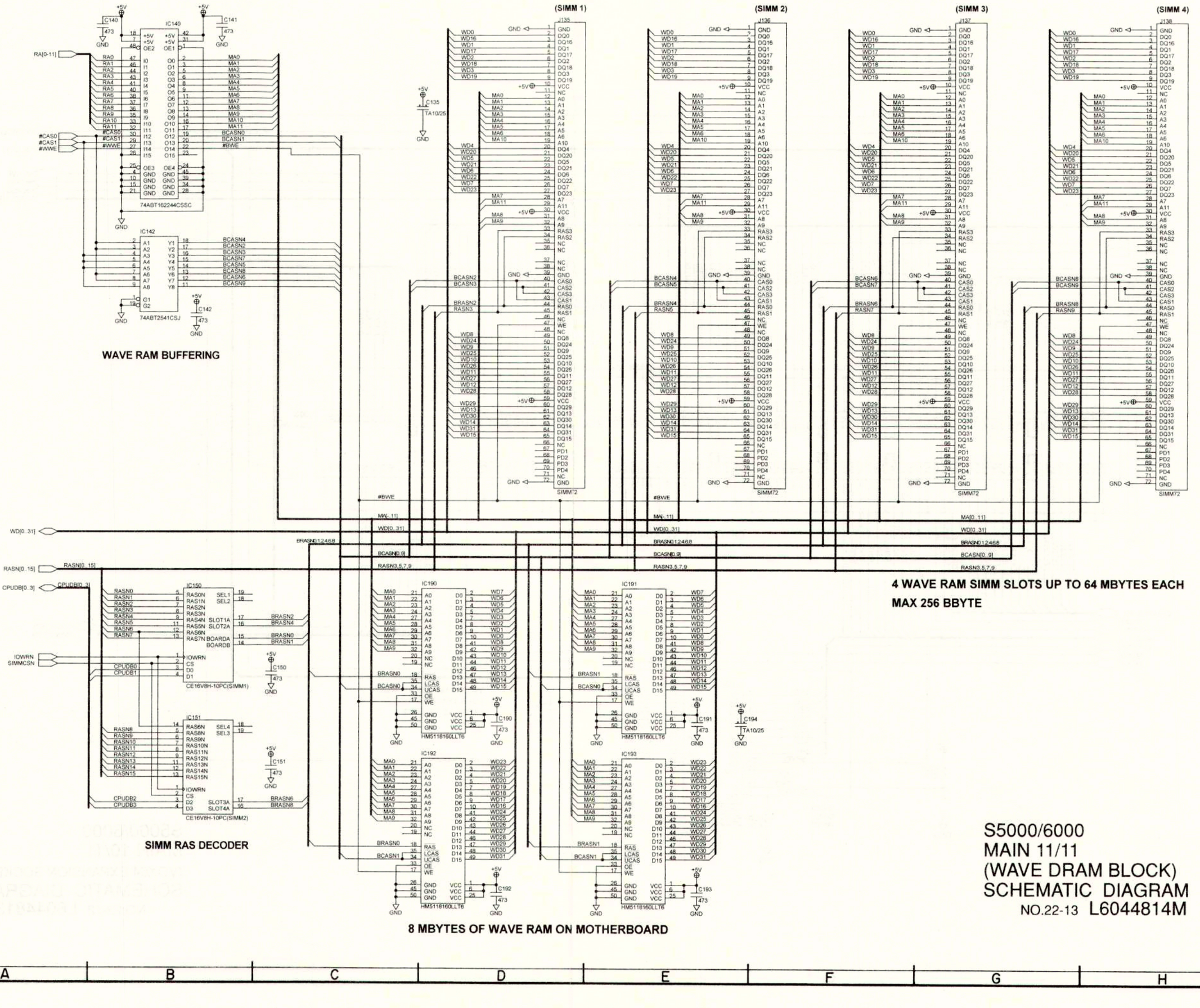
S5000/6000
MAIN 8/11
(I/O SOCKET)
SCHEMATIC DIAGRAM
NO.22-10 L6044811M



S5000/6000
MAIN 9/11
(VOX64 SOCKET)
SCHEMATIC DIAGRAM
NO.22-11 L6044812M



S5000/6000
MAIN 10/11
(VOX64 EXPANSION SOCKET)
SCHEMATIC DIAGRAM
NO.22-12 L6044813M



S5000/6000
MAIN 11/11
(WAVE DRAM BLOCK)
SCHEMATIC DIAGRAM
NO.22-13 L6044814M

PRINCIPAL PARTS LOCATION

ICs

IC5	D2
IC10	C,D1
IC11	C1
IC12	C,D1,2
IC13	C1
IC25	C1,2
IC26	B1,2
IC30	C3
IC31	C3,4
IC32	B3,4
IC40	B4
IC41	C4
IC42	B4
IC43	B4
IC44	C4
IC45	B4
IC46	B4
IC85	A1
IC86	E2
IC95	B3
IC110	A2
IC111	B3
IC112	A,B2
IC113	A2
IC114	B3
IC120	C2,3
IC121	C3
IC122	A1
IC123	A2
IC124	A1,2
IC125	A2
IC140	D3
IC142	D3,4
IC150	D4
IC151	D4
IC190	D4
IC191	D4
IC192	D3
IC193	D3
IC200	D3
IC210	C2
IC211	B2
IC212	C2
IC213	C2
IC214	C2
IC215	C2
IC216	D2
IC217	D1
IC218	B2
IC219	A1
IC221	B1
IC222	B2
IC223	B2
IC224	B,C2
IC225	B2
IC250	E1
IC251	D1
IC252	D1
IC253	D1
IC254	E1
IC255	D1
IC256	D1
IC257	D1
IC258	D,E1
IC259	E3
IC260	E3
IC261	E3,4
IC262	C1
IC263	E4
IC551	E3
IC552	E1
IC553	E1
IC554	E2
IC555	E4
IC650	A1
IC651	A1,2

TRANSISTORs

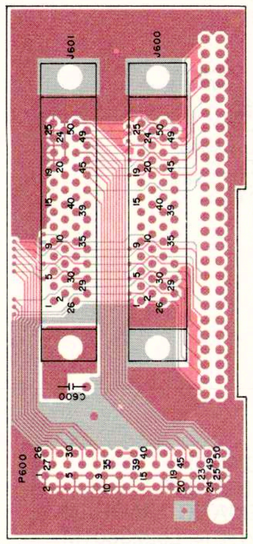
TR30	C3
TR40	B4
TR550	E2
TR551	D,E2
TR552	D,E2
TR553	D2

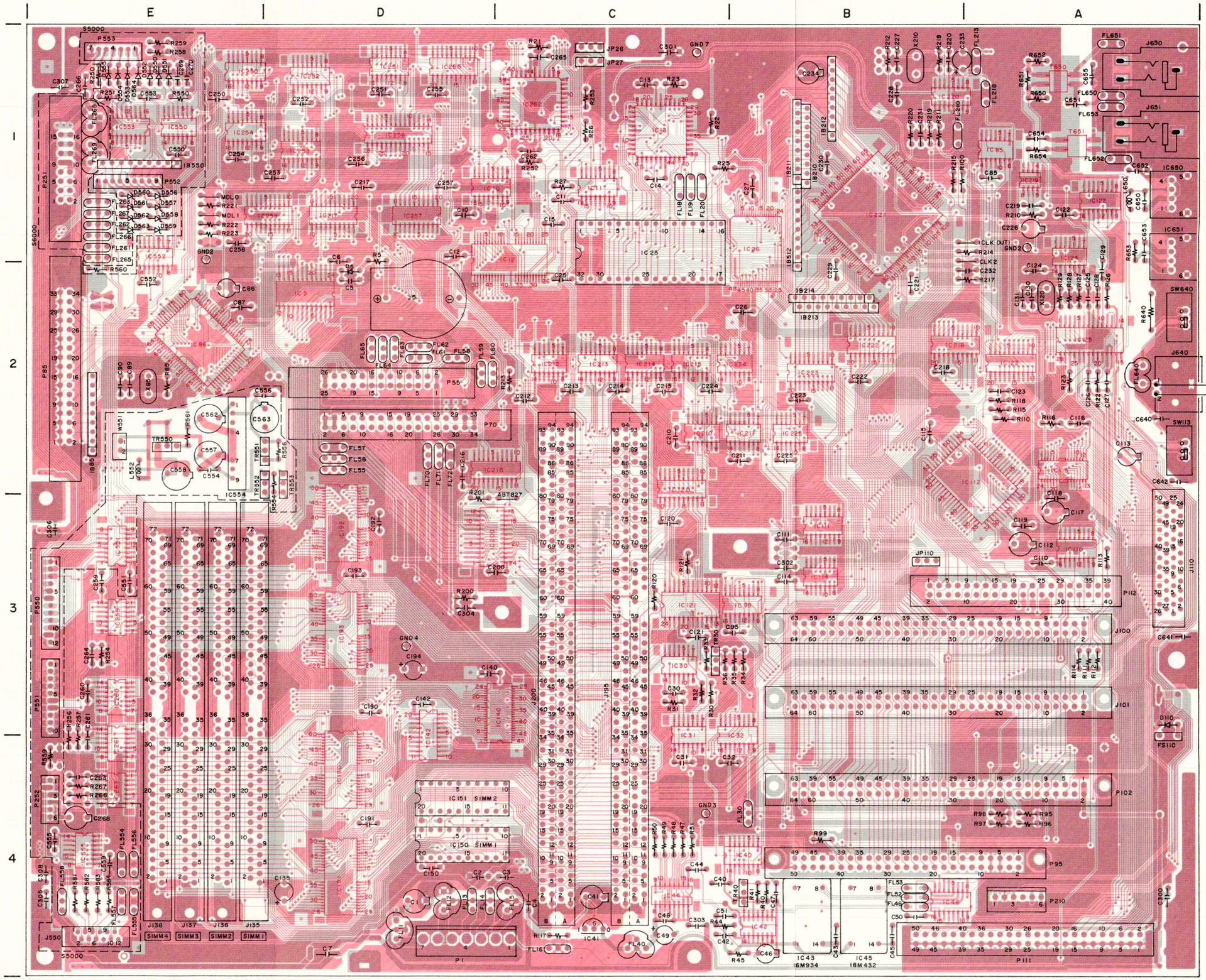
CONNECTORs

J5	D2
J100	A,B3
J101	A,B3
J110	A3
J112	A3
J135	E3,4
J136	E3,4
J137	E3,4
J138	E3,4
J195	C3
J200	C3
J550	E4
J640	A2
J650	A1
J651	A1
P1	D4
P55	D2
P70	D2
P85	E2
P95	B4
P102	A,B4
P111	A4
P112	A3
P120	A4
P210	A4
P251	E1
P252	E4
P550	E3
P551	E3
P552	E1
P553	E1

WIRE

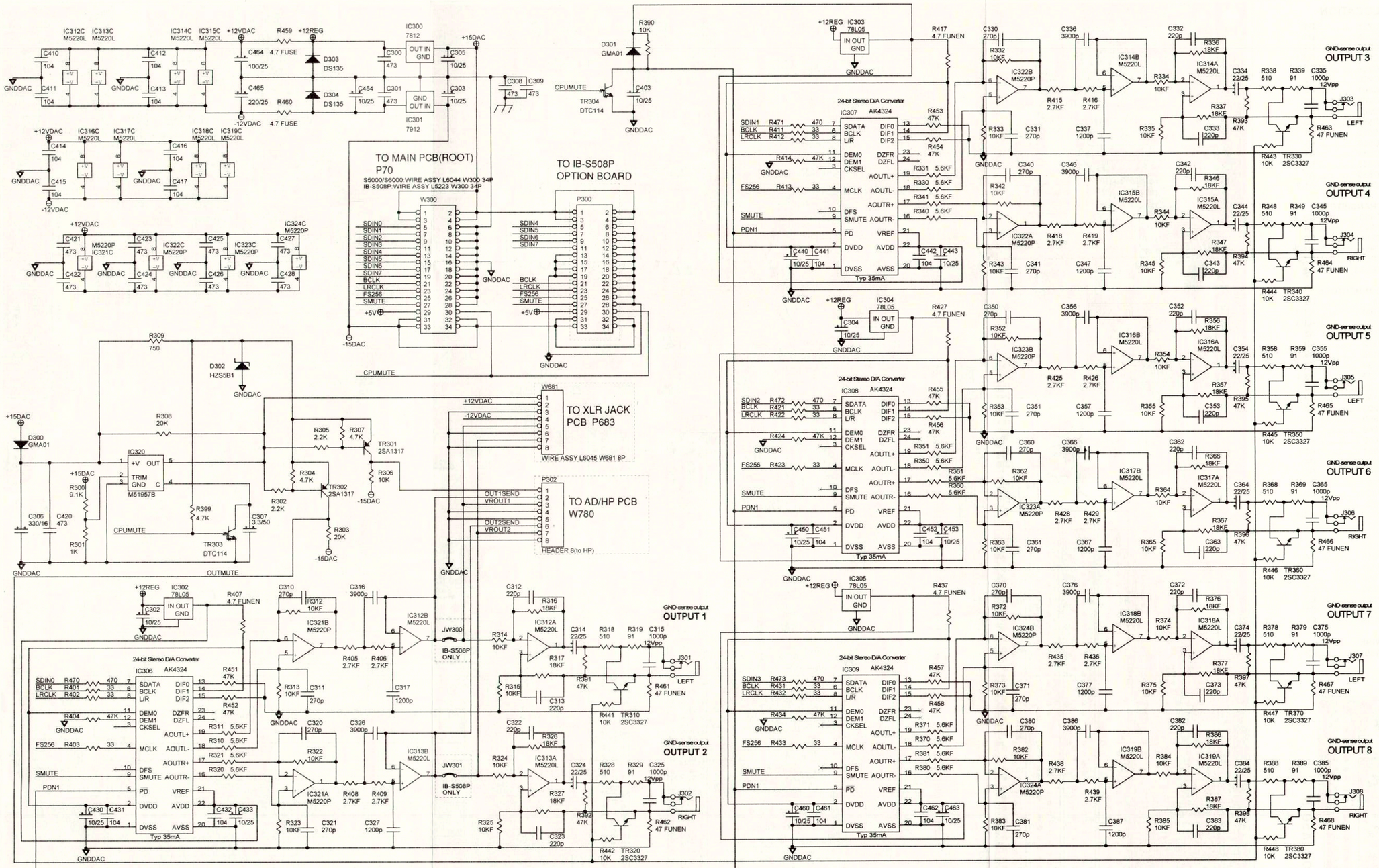
W551	E2





NOTE:
Parts differ depending on model number. Refer to schematic diagrams for pertinent parts information.

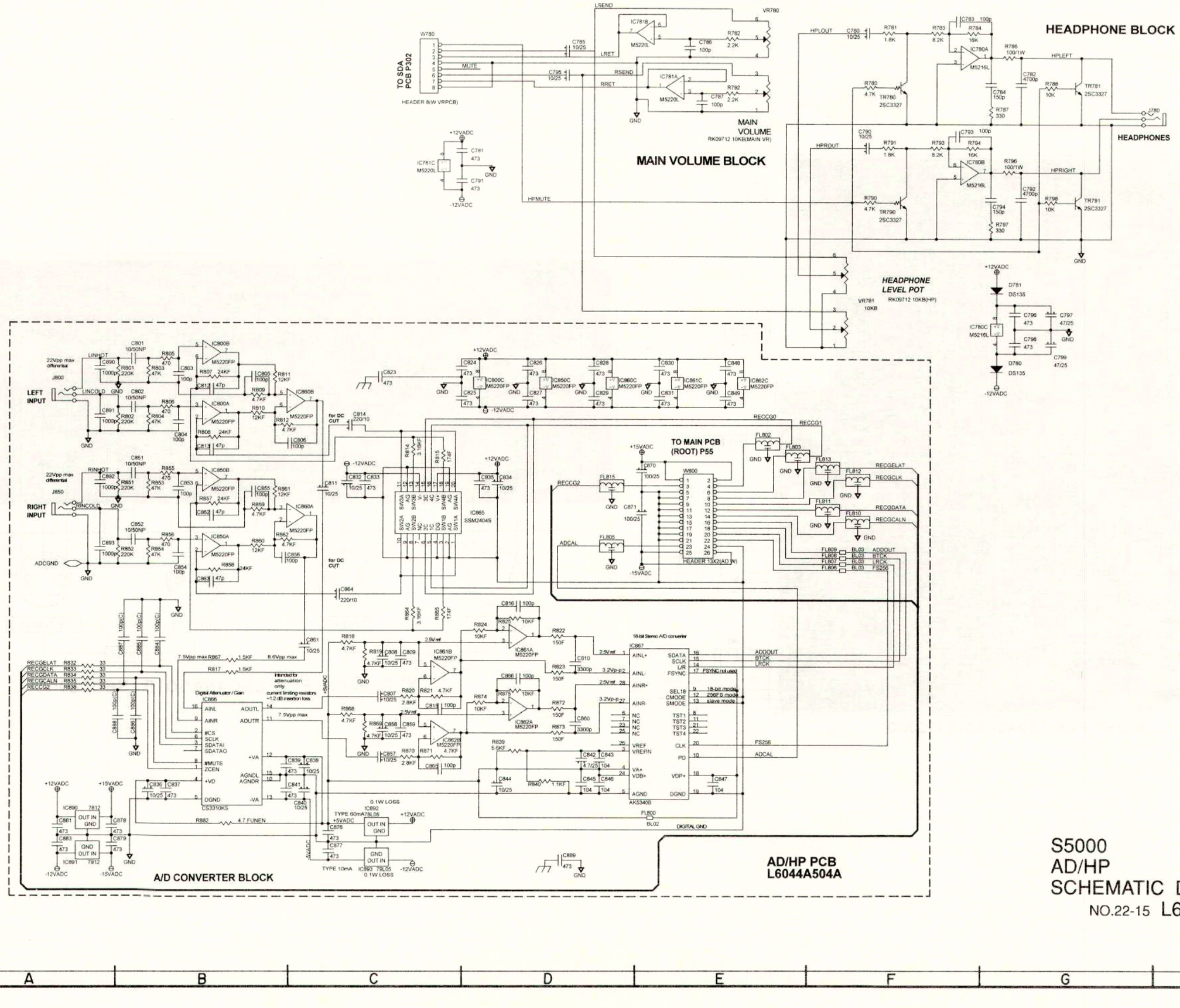
NOTE: This PC Board consists of four layers.
The inside two layers (sandwiched by the outside layers) are not shown in this PC Board layout.



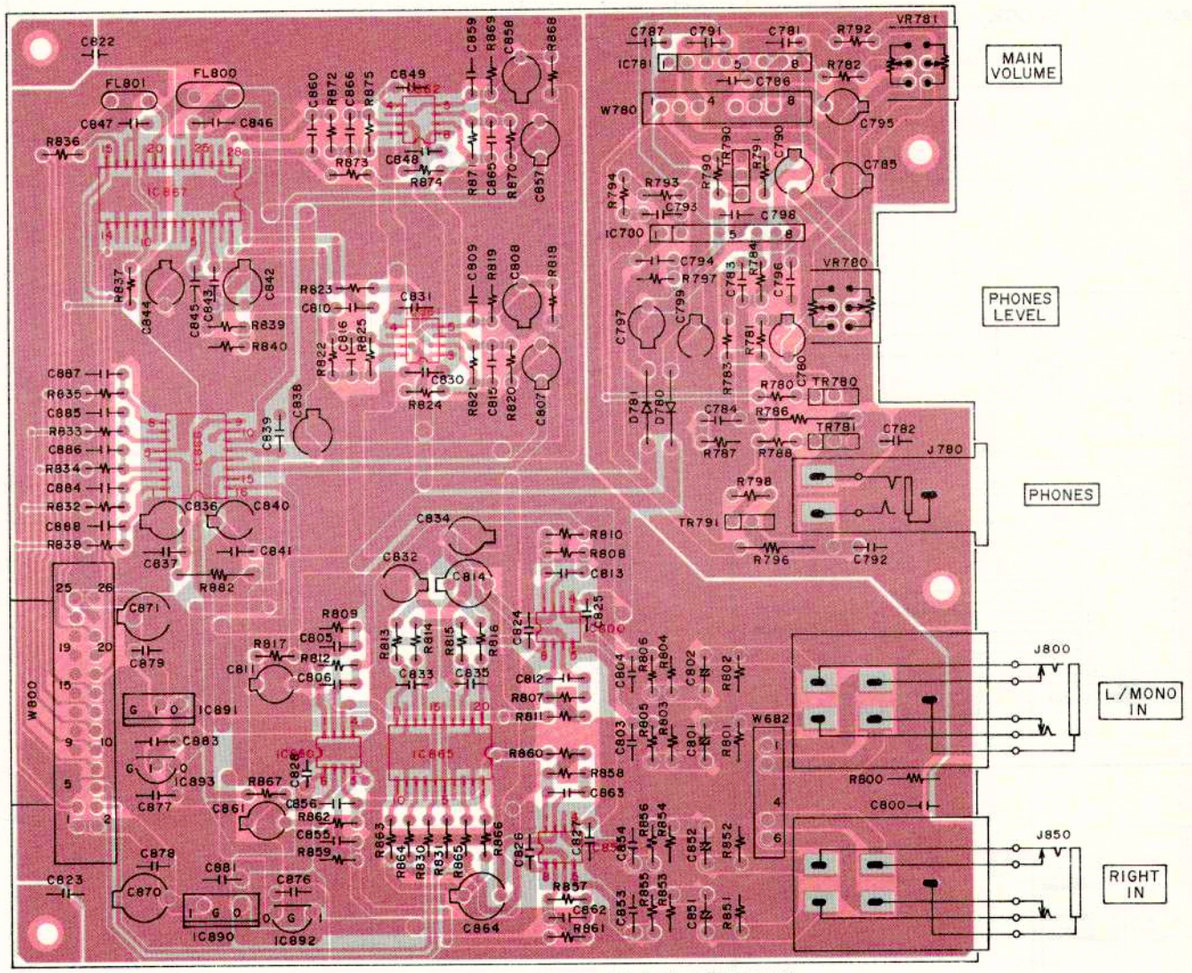
'98-5-12 SWAP FL400,401,402,403 to R470,471,472,473 470ohm
'98-5-6 SWAP AOUTL<=>AOUTR,AOUTL->L chan,AOUTR->R chan

SDA PCB L5223B5010(IB-S508P)

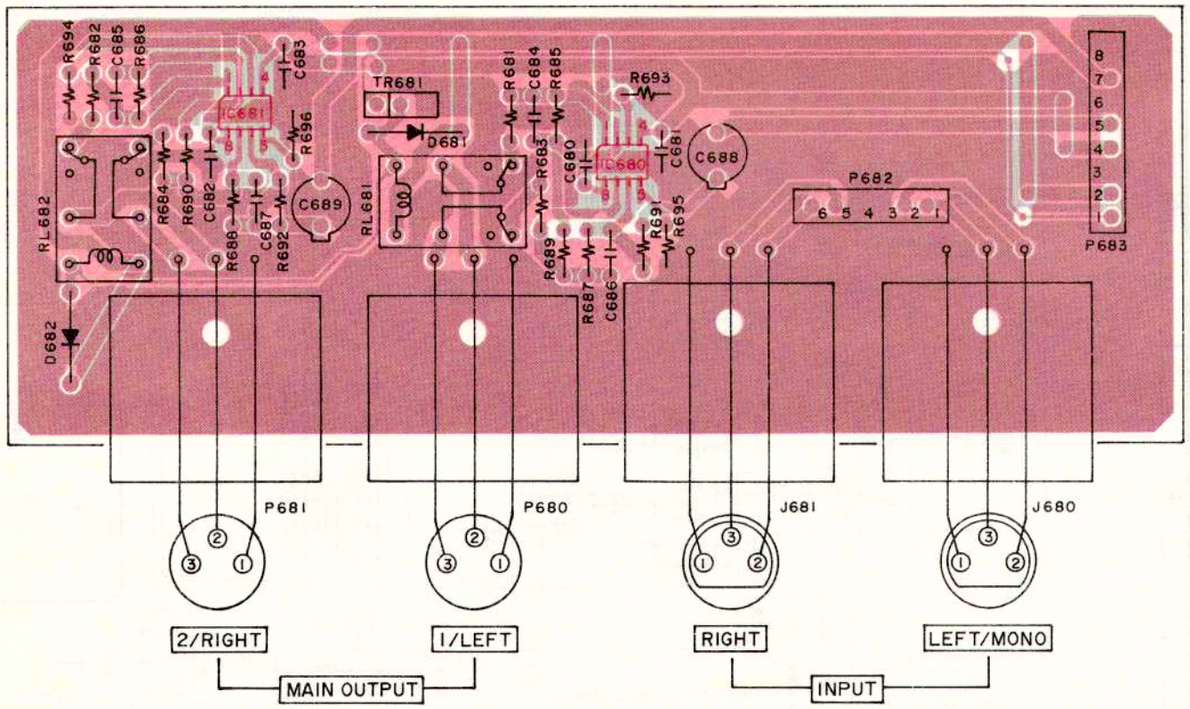
S5000/6000
SDA/IB-S508P
SCHEMATIC DIAGRAM
NO.22-14 L5223801M



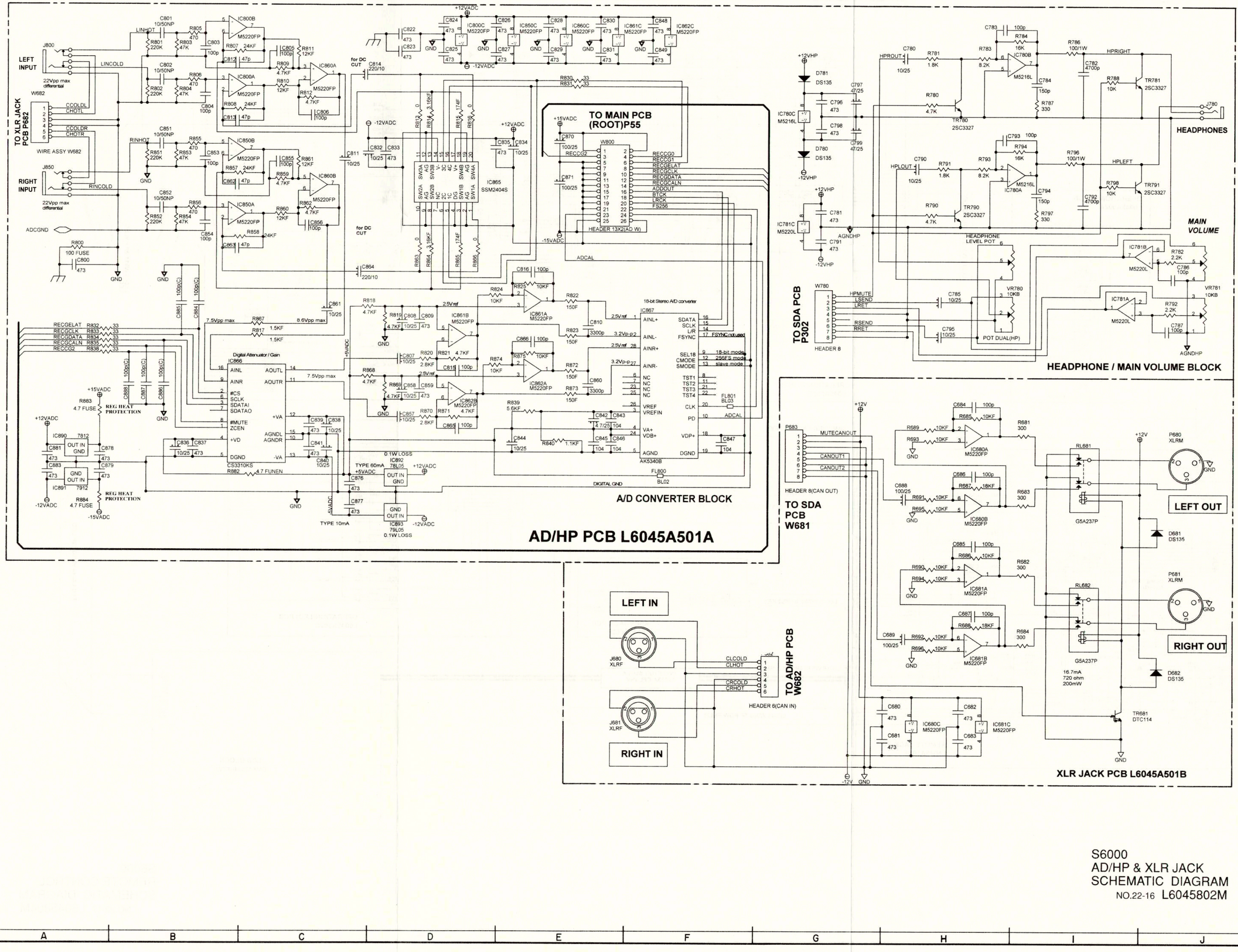
S5000
AD/HP
SCHEMATIC DIAGRAM
NO.22-15 L6044817M



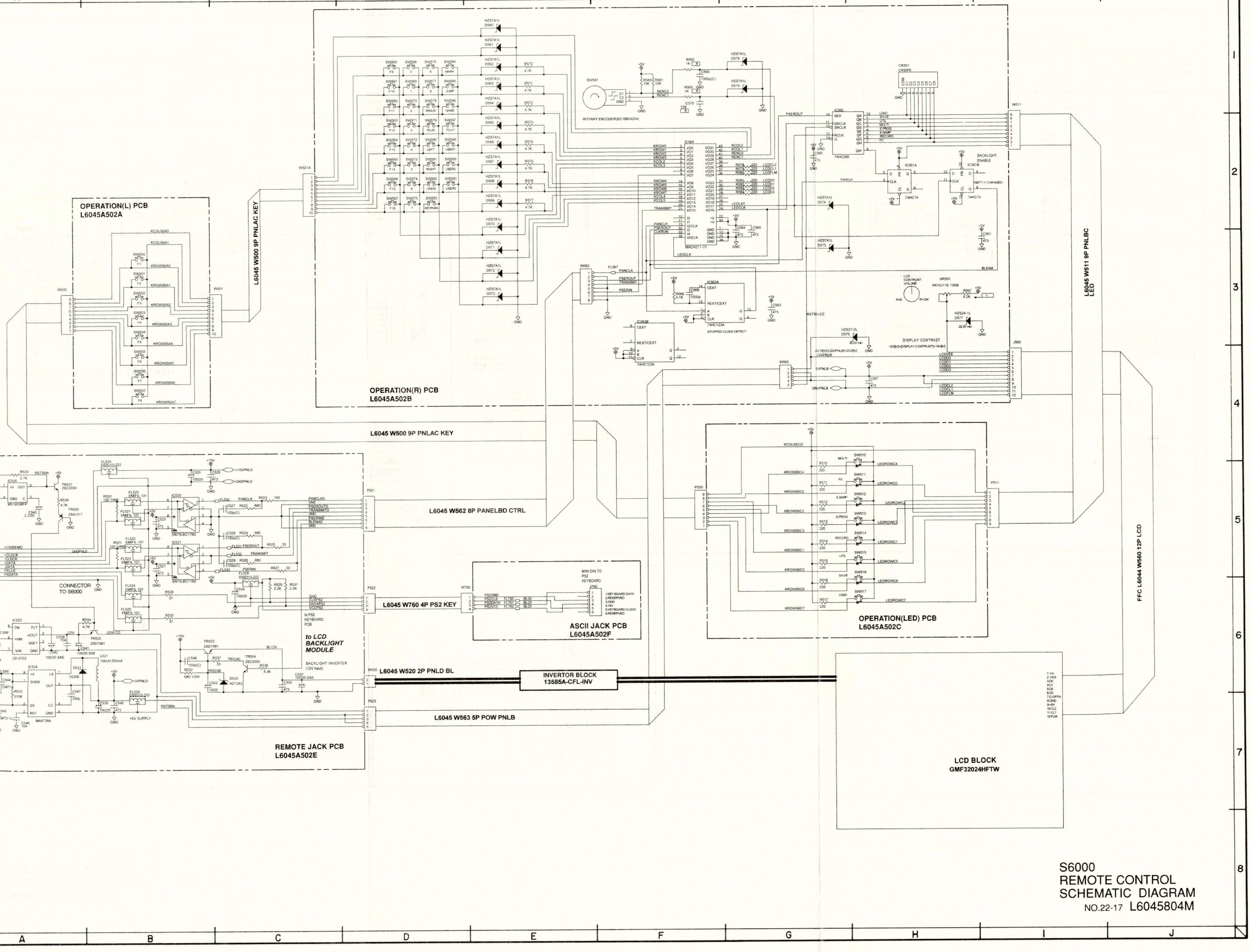
AD/HP PCB L6045A501A (S6000)

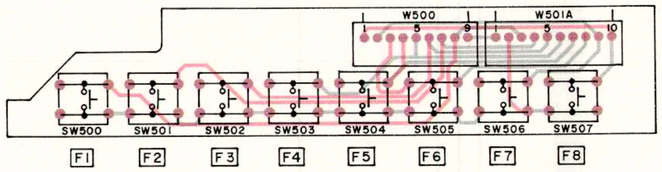


XLR JACK PCB L6045A501B (S6000)

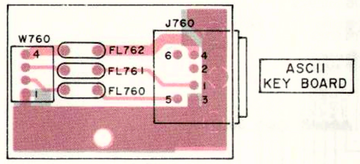


S6000
AD/HP & XLR JACK
SCHEMATIC DIAGRAM
NO.22-16 L6045802M

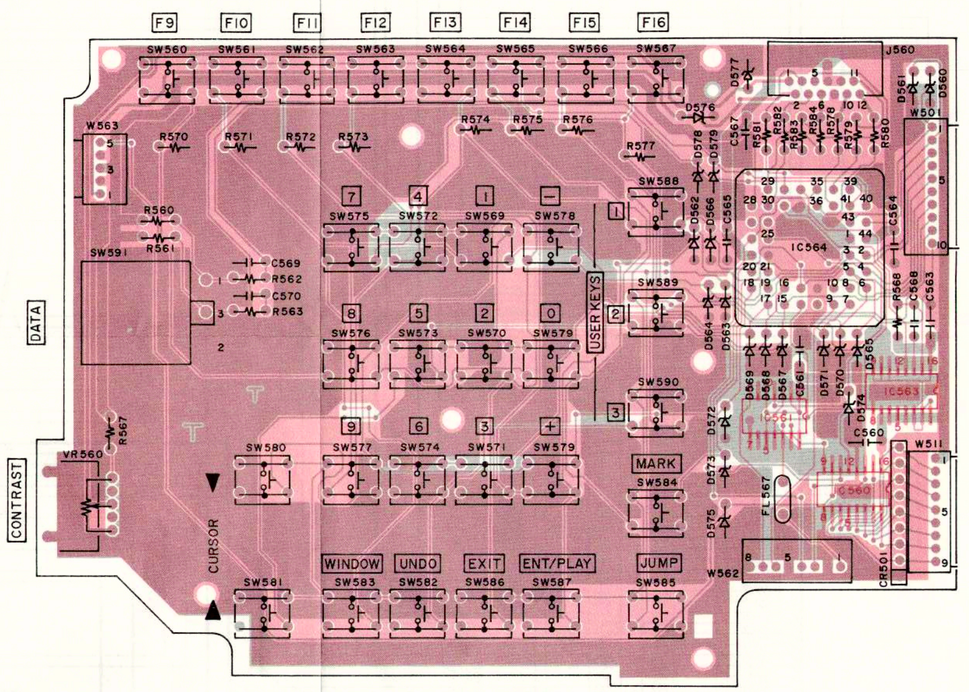

OPERATION(L) PCB
L6045A502A
OPERATION(R) PCB
L6045A502B
L6045 W500 9P PNLAC KEY
L6045 W511 9P PNLBC LED
L6045 W562 8P PANELBD CTRL
L6045 W760 4P PS2 KEY
L6045 W520 2P PNLD BL
L6045 W563 5P POW PNLB
ROTARY ENCODER(EC16B4204)
CONNECTOR TO S6000
to LCD BACKLIGHT MODULE
to PS2 KEYBOARD PCB
INVERTOR BLOCK 13585A-CFL-INV
REMOTE JACK PCB
L6045A502E
ASCII JACK PCB
L6045A502F
OPERATION(LED) PCB
L6045A502C
FFC L6044 W560 12P LCD
LCD BLOCK
GMF32024HFTW
S6000
REMOTE CONTROL
SCHEMATIC DIAGRAM
NO.22-17 L6045804M



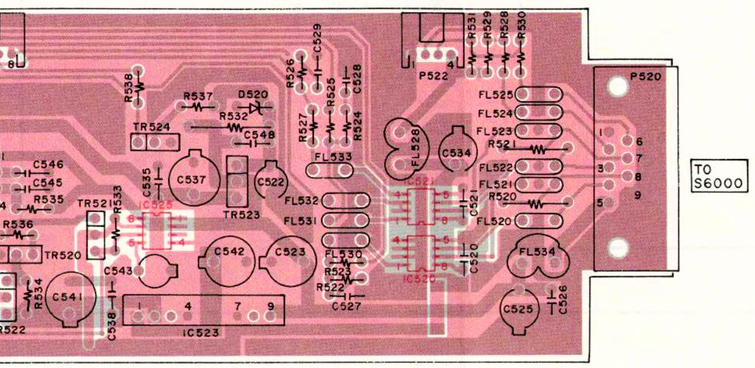
OPERATION (L) PCB L6045A502A (S6000)



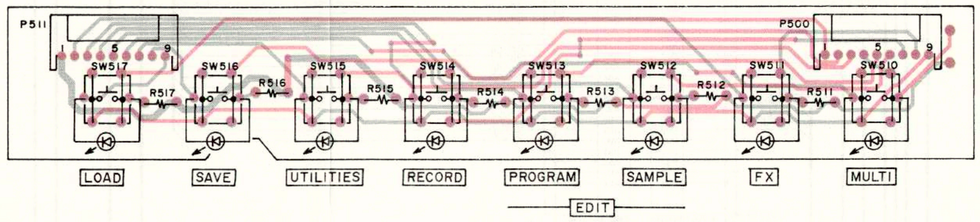
ASCII JACK PCB L6045A502F (S6000)



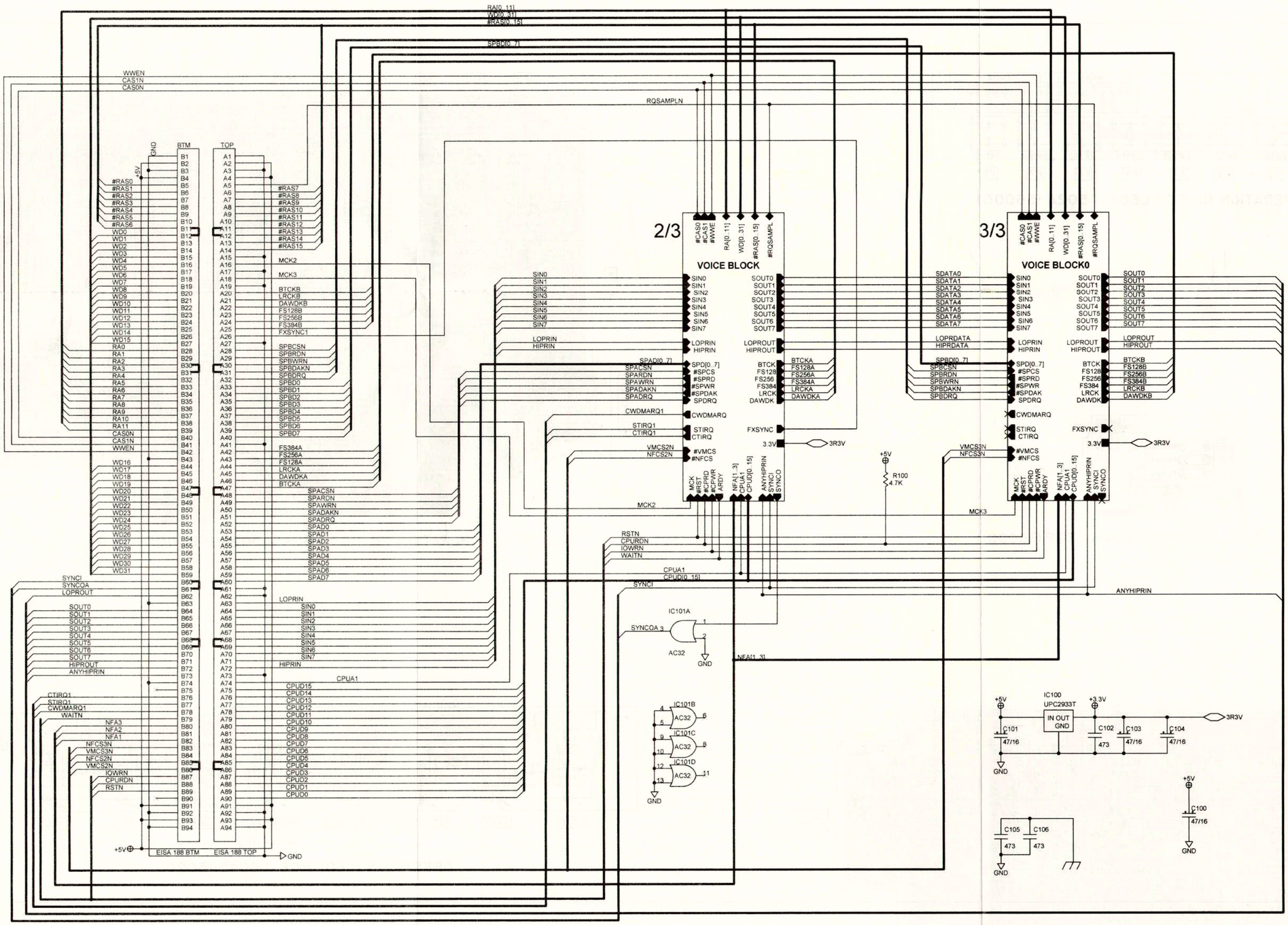
OPERATION (R) PCB L6045A502B (S6000)



REMOTE JACK PCB L6045A502E

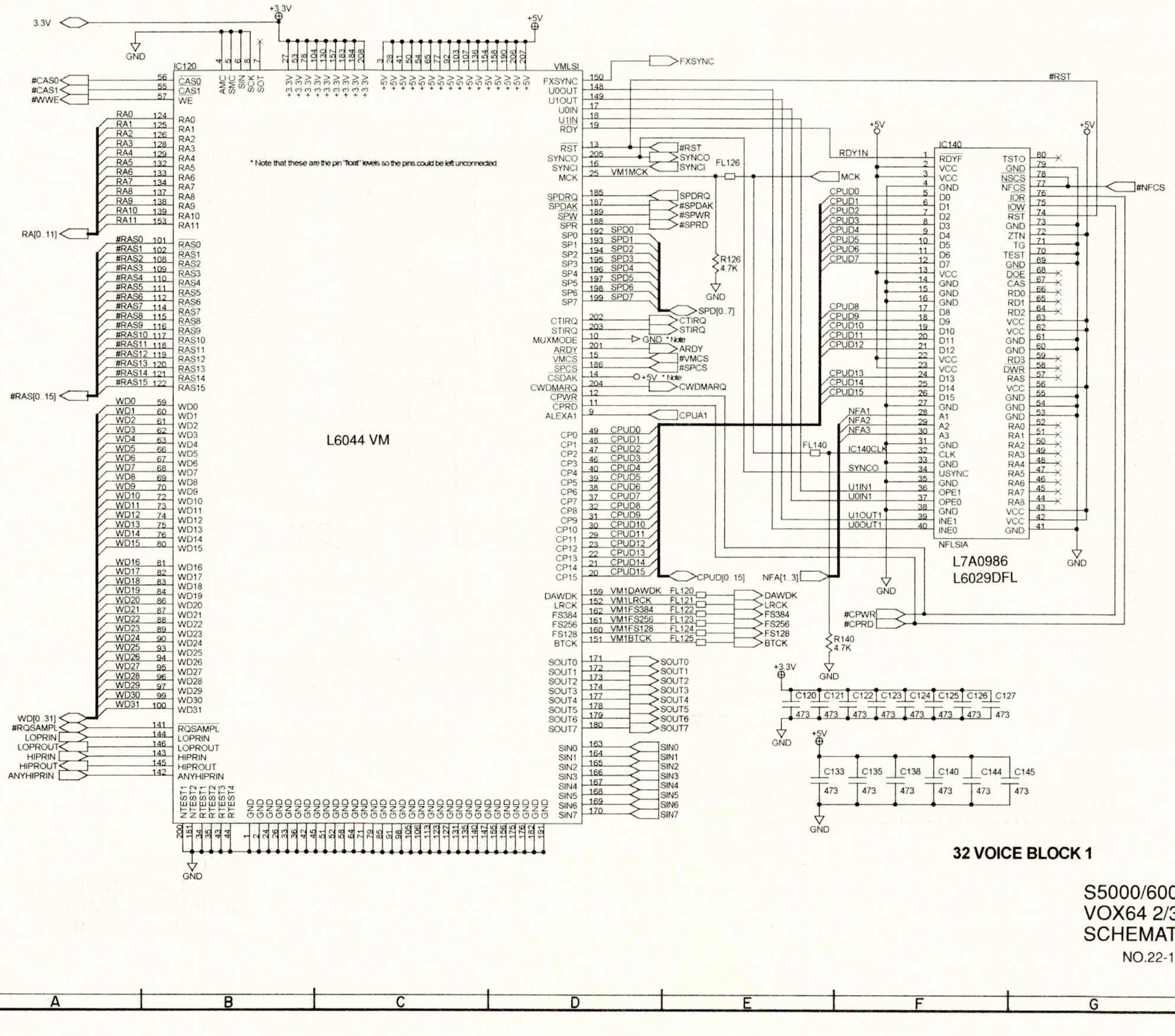


OPERATION (LED) PCB L6045A502C

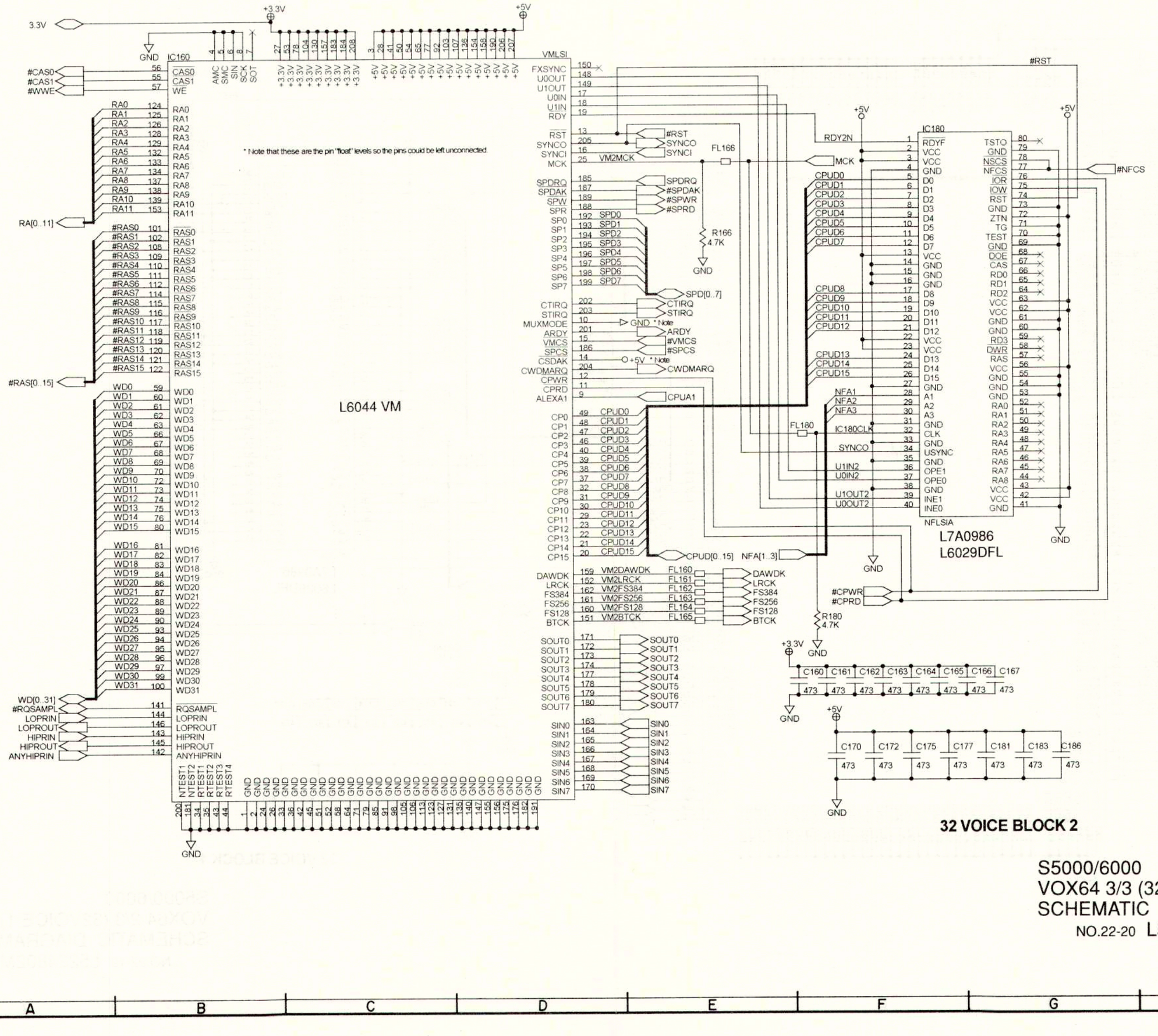


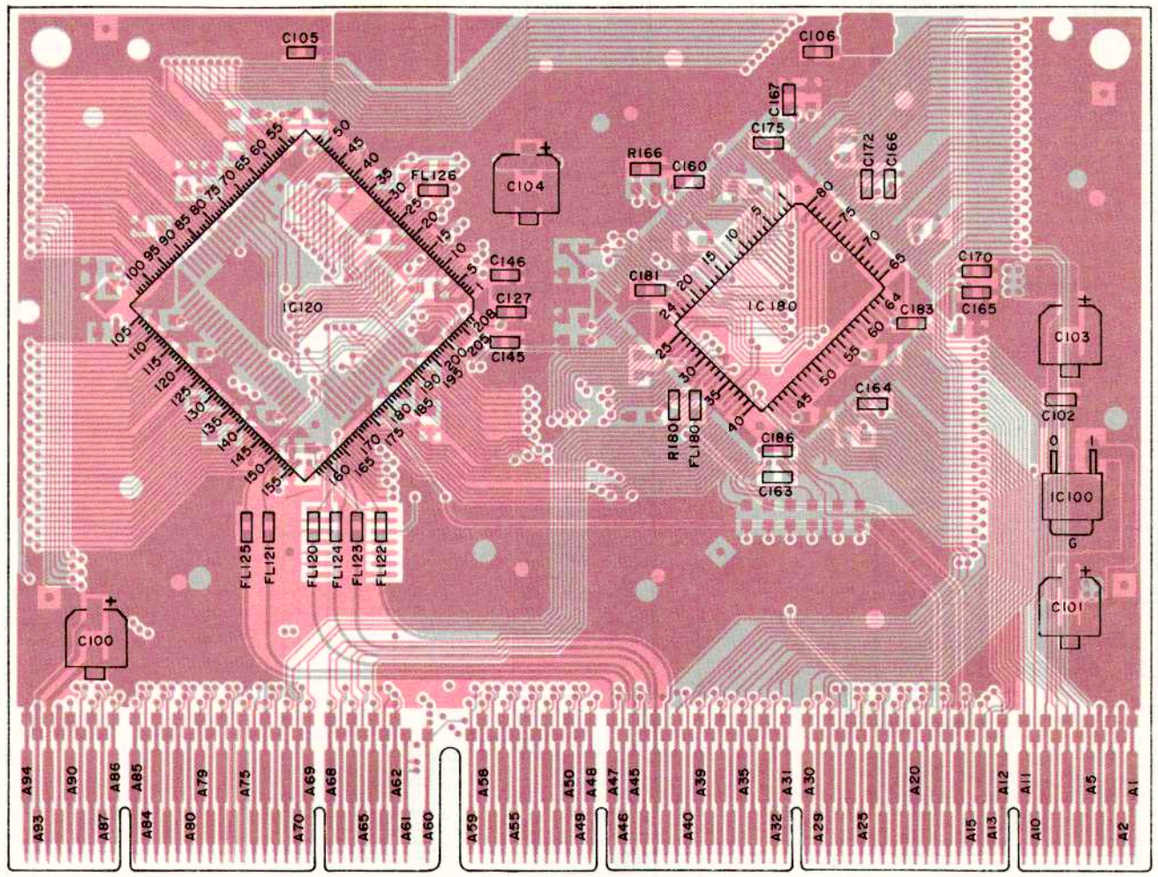
VOX PCB (VOX64)
L5224B5010

S5000/6000
VOX64 1/3
SCHEMATIC DIAGRAM
NO.22-18 L5224801M

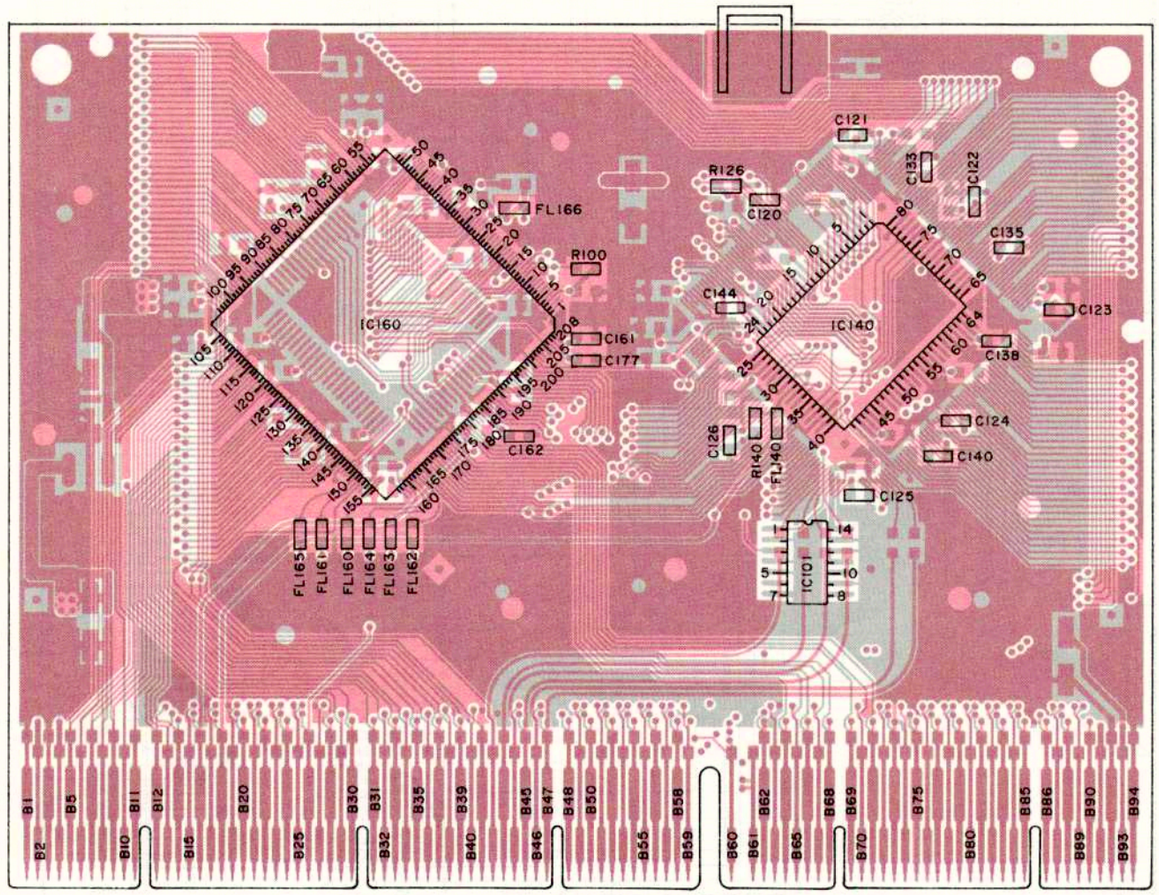


S5000/6000
VOX64 2/3 (32VOICE 1)
SCHEMATIC DIAGRAM
NO.22-19 L5224802M


L6044 VM
* Note that these are the pin "float" levels so the pins could be left unconnected.
L7A0986
L6029DFL
32 VOICE BLOCK 2
S5000/6000
VOX64 3/3 (32VOICE 2)
SCHEMATIC DIAGRAM
NO.22-20 L5224803M



VOX PCB (VOX 64) L5224B5010 (TOP)



VOX PCB (VOX 64) L5224B5010 (BOTTOM)

NOTE: This PC Board consists of six layers.
The inside four layers (sandwiched by the outside layers) are not shown in this PC Board layout.

EFFECTS OPTION BOARD

TO MAIN PCB(8/11) P95

J1 — VCC, VCC, VCC, VCC, GND, GND, GND, GND, WSENCE, DIBCKI, DILRCKI, DIBCKO, DILRCKO, FXCS, DIN1, DIN0, GND, D8, D9, D10, D11, D12, D13, D14, D15, D0, D1, D2, D3, D4, D5, D6, D7, GND, IORD, IOWR, ARDY, RST, DOUT, A/D, GND, DOLRCK, DOBCK, GND, FS256, FS384, FXSYNC, GND, MCK, GND

+5V — C11 10/25 — GND

WSENSE, DIBCKI, DILRCKI, DIBCKO, DILRCKO, FXCSN, DIN1, DIN0, D8, D9, D10, D11, D12, D13, D14, D15, D0, D1, D2, D3, D4, D5, D6, D7, IORDN, IOWRN, WAIT, RSTN, DOUT, ADR_DATAN, DOLRCK, DOBCK, FS256, FS384, FXSYNC, FS768

D[0..15]

FL1 BL03 FS768B

FL2 BL03 FS256B

FL3 BL03 FS384B

IC7 — FXLSI — L7A1414 L6028DFX

VCC, GND, TE, SCTE, MTES, RWEN, W/R, R/W, RD, VCC, GND, D0–D15, VCC, GND, B8/B16, LH/HL, DH/DL, A/D, ADSTRB, ADSTRB, ZTN, GND, VCC, VCC, GND, USYNC, SD1IN, SD0IN, DIN1, DIN0, DIBCKIA, DIBCKIB, DILRCKI, GND, FS768M, VCC, GND, SD1OUT, SD0OUT, DIBCKO, DIBCKO, DILRCKO, GND, VCC, DILRCKO, DOUT, DOBCK, DOLRCK, FS256, GND, GND, VCC, FS256, GND, MQ0, MQ0, V0V16, MA17, MA16, MA15, MA17, GND, VCC

VCC, GND, CS2, CS1, CS1, CS0, CS0, WAITOR, GND, VCC, NC, BCK, WSENSE, RESET, GND, VCC, WAIT, MD0–MD23, GND, VCC, MD6, MD7, MD8, MD9, MD10, GND, VCC, MD11, MD12, MD13, MD14, MD15, MD16, GND, VCC, VCC, GND, TESTOUT, GND, MD17, MD18, MD19, MD20, MD21, MD22, MD23, GND, VCC, MOE, MWE, GND, VCC, MA0–MA16, GND, VCC

MOEN, MWEN

GND — GND — MA17

JP1 — 1 2 3 — GND

"1-2 short and 2-3 cut" for full memory

EFFECTOR(EB20FX) PCB
L5225B5010

+5V — C7 473, C8 473, C9 473, C10 473 — GND — FOR FXLSI

MD[0..23]

IC1, IC2, IC3 — UPD431000AGW-85L

A0–A16, D0–D7, $\overline{OE}$, $\overline{WE}$, NC, VCC, GND, $\overline{CS1}$, $\overline{CS2}$

+5V — C1 473 — GND

MA[0..16]

CS1_IC123

IC4, IC5, IC6 — UPD431000AGW-85L

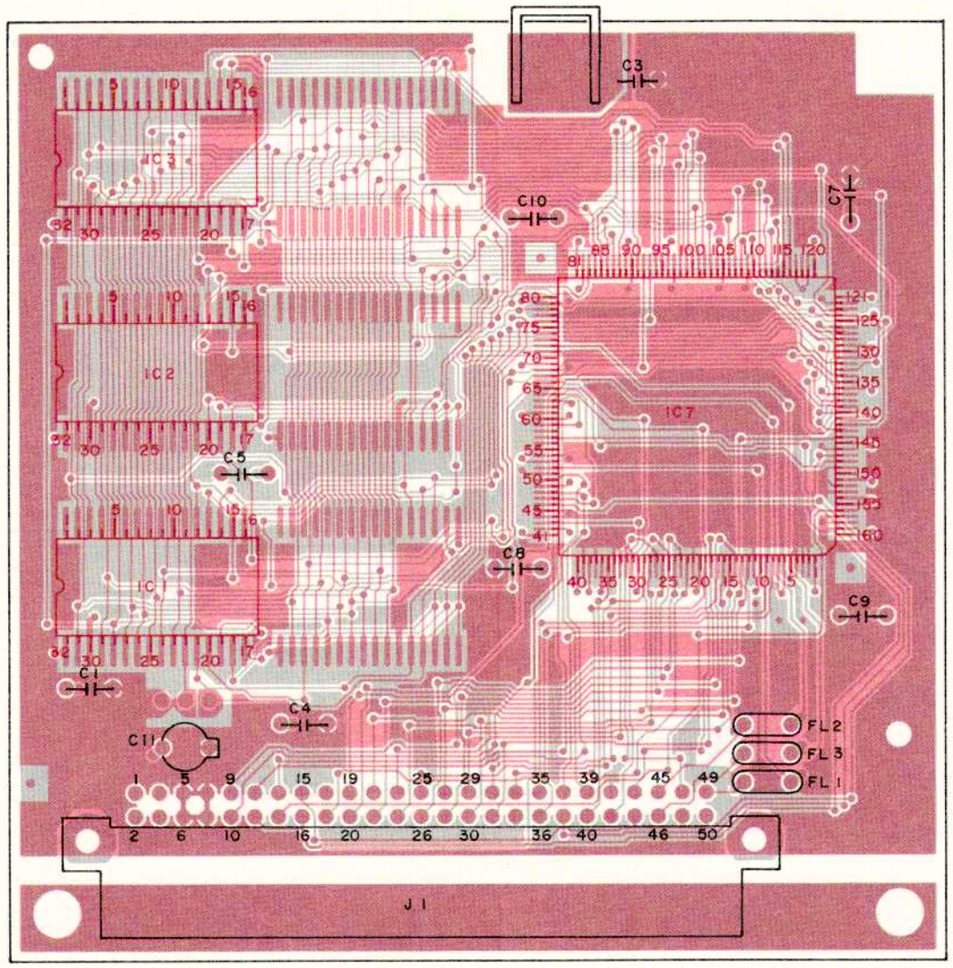
+5V — C4 473 — GND

+5V — C5 473 — GND

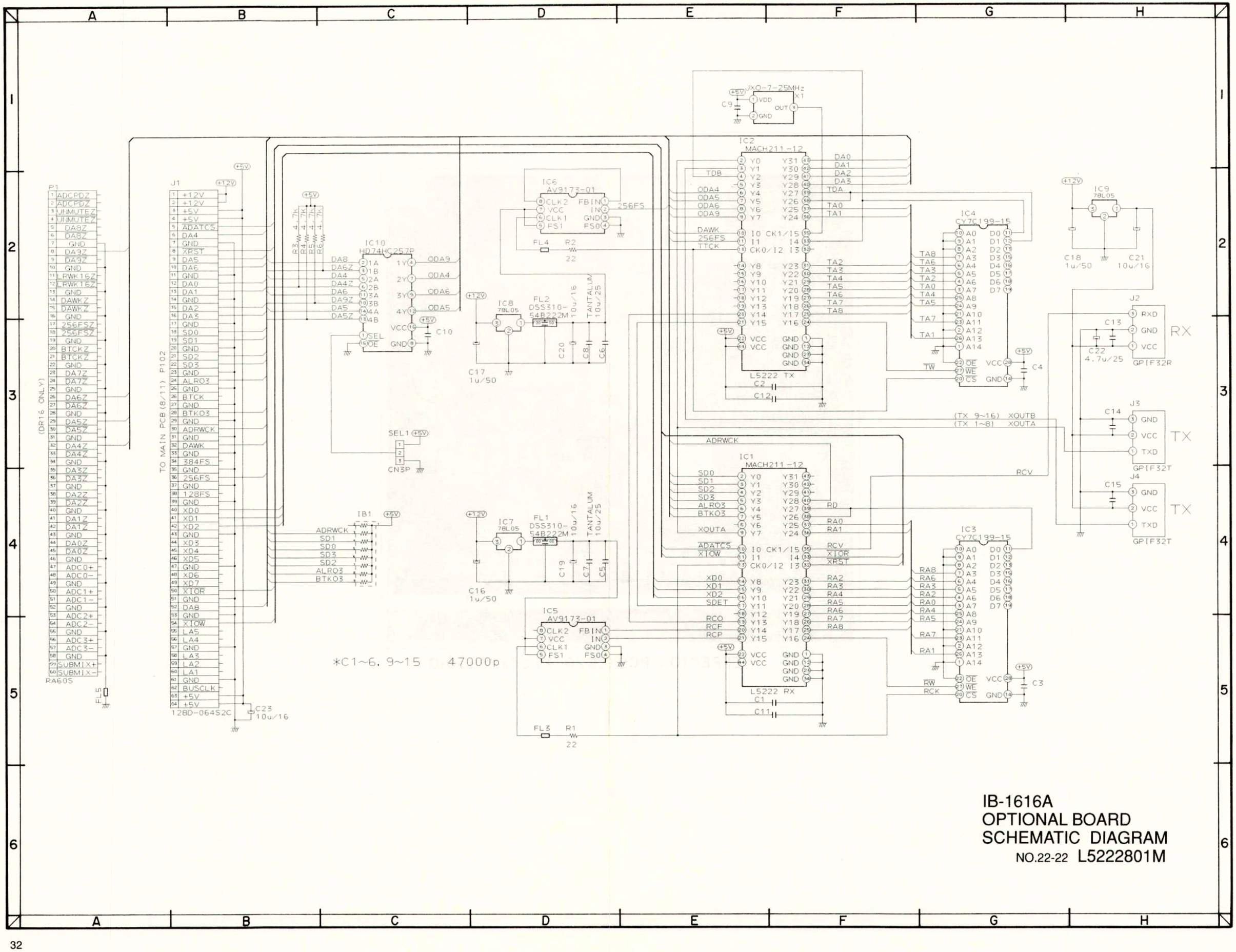
+5V — C3 473 — GND

Included for full effects memory

EB20
OPTIONAL BOARD
SCHEMATIC DIAGRAM
NO.22-21 L5225801M



EFFECTOR PCB (EB20FX) L5225B5010



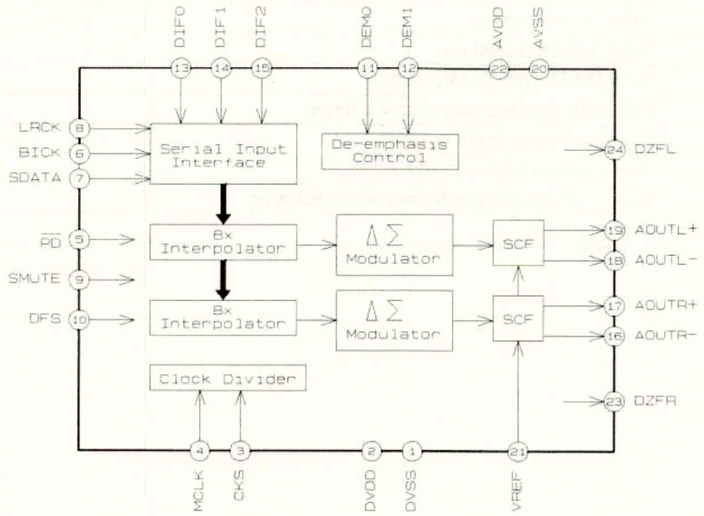
IB-1616A
OPTIONAL BOARD
SCHEMATIC DIAGRAM
NO.22-22 L5222801M

INFORMATION of ICs

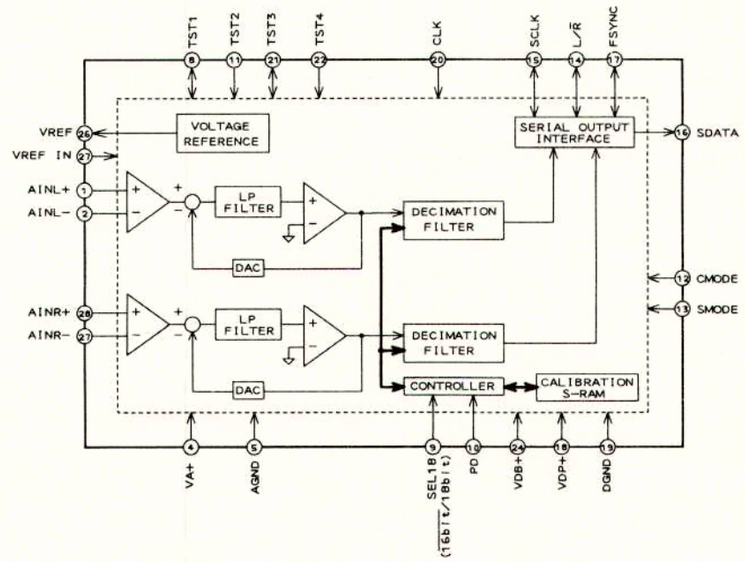
NAME OF IC	FUNCTION
AK4324	24 bit dual D/A converter with 128 fs over-sampling digital filter
AK5340B	18 bit dual A/D converter with 64 fs over-sampling digital filter
AV9154A-04	Frequency Generator with clock doubler
AV9172-03	Low skew output buffers
AV9173-01	Video generator locked PLL
BH9595FP-Y	Active terminator
CE16V8H-10PC	SIMM RAS decoder
CE-0703	DC-DC converter (12 V to –24 V)
CS3310KS	Dual digital volume controller
CS8402A	Digital audio transmitter
CS8412	Digital audio receiver
CY7C199-15	32 k x 8 bit S-RAM
CY7C199-20VC	32 k x 8 bit S-RAM
CXD1185AQ	SCSI controller
E28F800B5-T70	1 M x 8 bit CPU F-ROM
L7A0986	Digital filter
L7A1414 (L6028 DFX)	Digital filter
L6044 VM	32 voice DSP
HM5118160LLT6	1 M x 16 bit DRAM
KU80386EXTC-33	16 bit CPU
M2DB-16M934	44.1 kHz VCO
M2DB-18M432	48.0 kHz VCO
M5216L	High output level OP-AMP
M5220L/P	Dual low noise OP-AMP
M51953FP	System reset pulse generator
M51957B	System reset pulse generator
MACH211-10DRC	CPU D-RAM control PLD
MACH211-10PNLC	Operation control PLD
MACH211-12 (L5222 RX)	ADAT signal receive PLD
MACH211-12 (L5222 TX)	ADAT signal transmit PLD
MAX738A	DC-DC converter (12 V to 5 V)
PC910	Photo coupler
RTC-6593	Real time clock /Non-volatile RAM
SN75LBC176D	Differential bus transceiver
SSM2404S	Quad analog switches
UPC2933T	3.3V regulator
UPD72068GF	Floppy disk drive controller
UPD431000AGW-85L	1 Mbit static RAM
27C080-150	1 M x 8 bit CPU EP-ROM
74ABT2541CSJ	Octal 3-state buffers
74ABT162244CSSC	16 bit 3-state buffers
74AC138	3 to 8 line decoder
74AC153	Dual 4-input multiplexers
74AC245	Octal 3-state BUS transceivers
74ACT841SC	10 bit transparent latch
74HC02	Quad 2-input NOR gates
74HC04	Hex inverters
74HC32	Quad 2-input OR gates
74HC74	Dual D-FFs with preset and clear
74HC123A	Dual retriggerable monostable multivibrators
74HC126	Quad 3-state buffers
74HC139	Dual 2 to 4 demultiplexers
74HC153	Dual 4-input multiplexers
74HC157	Quad 2-input multiplexers
74HC164	8 bit serial-in/parallel-out shift register
74HC166	8 bit shift register
74HC257P	Quad 2-channel 3-state multiplexer
74HC299	8 bit shift register

NAME OF IC	FUNCTION
74HC541	Octal 3-state buffers
74HC573	Octal 3-state D-latches
74HC574	Octal D-FFs with 3-state output
74HC595	8 bit shift registers with output latches
74HC4040	12-stage binary ripple counter
74HC4046AD	Phase locked loop with VCO
74HC4053	Triple 2-channel multiplexers/demultiplexers
78L05	+5 V regulator

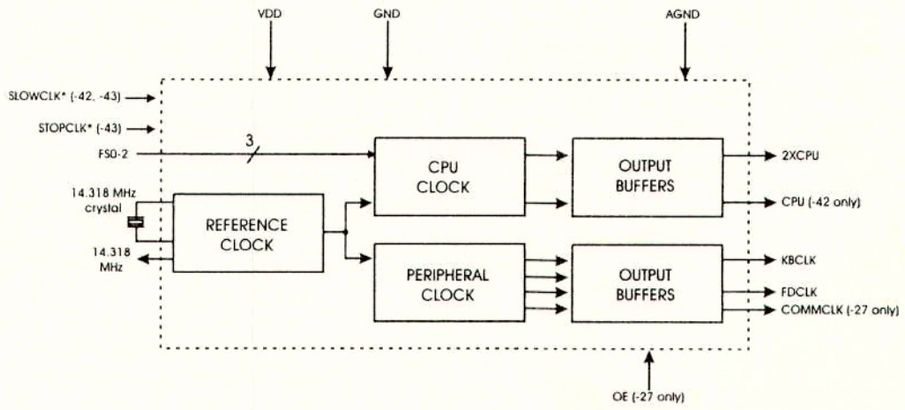
AK4324 (24 bit dual D/A converter with 128 fs over-sampling digital filter)



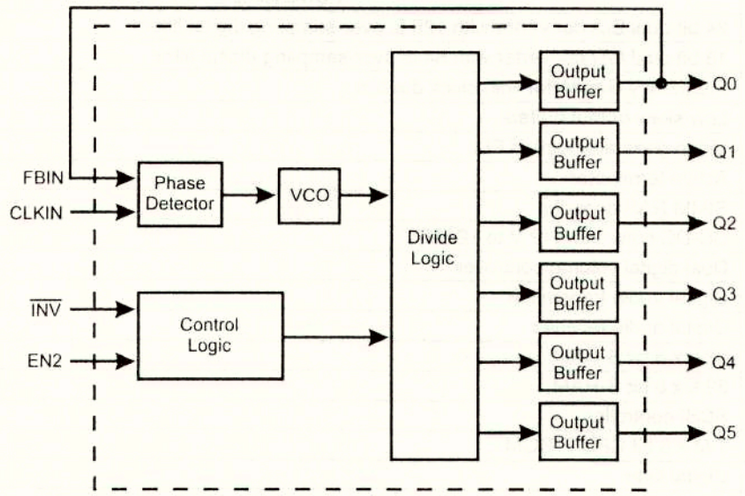
AK5340B (18 bit dual A/D converter with 64 fs over-sampling digital filter)



AV9154A-04 (Frequency Generator with clock doubler)



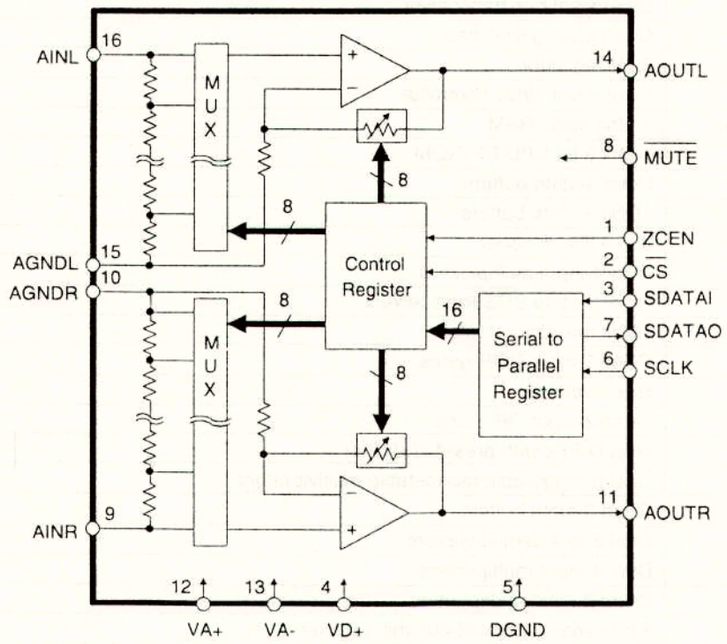
AV9172-03 (Low skew output buffers)



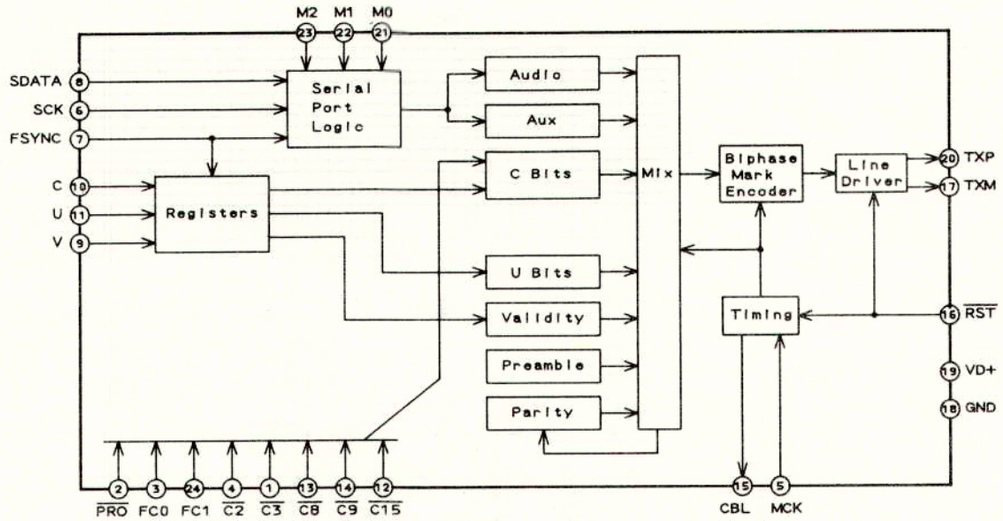
AV9173-01 (Video generator locked PLL)

PIN No.	PORT NAME	I/O	FUNCTION
1	FBIN	I	Feedback input.
2	IN	I	Input for reference sync pulse.
3	GND	–	Ground.
4	FS0	I	Frequency select 0 input.
5	OE	I	Output enable.
6	CLK1	O	Clock output 1.
7	VDD	–	+5 V power supply.
8	CLK2	O	Clock output 2.

CS3310KS (Dual digital volume controller)

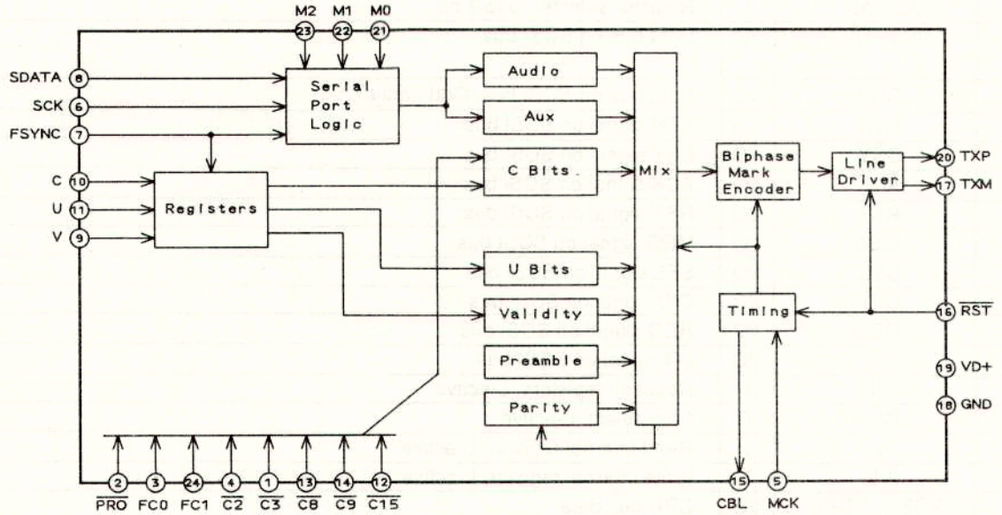


CS8402A (Digital audio transmitter)



PIN No.	PORT NAME	I/O	FUNCTION
1	$\overline{C7}/\overline{C3}$	I	C7 is the inverse of channel status bit 7 (in professional mode). C3 is the inverse of channel status bit 3 (in consumer mode).
2	$\overline{PRO}$	I	Select the professional mode (low) and consumer mode (high). C1 is the inverse of channel status bit 1 (in professional mode).
3	$\overline{C1}$/FC0	I	FC0 and FC1 are encoded versions of channel status bits 24 and 25 (bits 0 and 1 of byte 3). When FC0 and FC1 are both high, CD mode is selected.
4	$\overline{C6}/\overline{C2}$	I	C6 is the inverse of channel status bit 6 (in professional mode). C2 is the inverse of channel status bit 2 (in consumer mode).
5	MCK	I	Master clock input pin.
6	SCK	I	Serial clock input pin.
7	FSYNC	I	Frame sync input pin.
8	SDATA	I	Audio data serial input pin.
9	V	I	Validity bit serial input port.
10	C/SBF	I	C is the channel status serial input port (in professional & consumer modes). This pin inputs the CD subcode frame clock (CD mode).
11	U	I	User bit serial input port.
12	$\overline{C9}/\overline{C15}$	I	C9 is the inverse of channel status bit 9 (in professional mode). C15 is the inverse of channel status bit 15 (in consumer mode).
13	EM1/$\overline{C8}$	I	Emphasis 0,1 (In professional mode, EM0 and EM1 encode channel status bits 2,3 and 4).
14	EM0/$\overline{C9}$		C8 and C9 are inverse of channel status bits 8 and 9. In professional and consumer modes, the channel status block output is high
15	CBL/$\overline{SBC}$	O	for the first four bytes of channel status. In CD mode, this pin outputs the subcode bit clock.
16	$\overline{RST}$	I	Master reset pin.
17	TXN	O	RS422 compatible differential line driver.
18	GND	–	Ground pin.
19	VD+	–	Positive side of the power supply pin.
20	TXP	O	RS422 compatible differential line driver.
21 - 23	M0 to M2	I	Serial port mode select pins. (Select the format of F SYNC and the sample edge of SCK with respect to SDATA.)
24	CRE/FC1	I	If CRE is high, the channel status local sample address and reliability flag are internally generated (in professional mode). FC0 and FC1 are encoded versions of channel status bits 24 and 25 (bits 0 and 1 of byte 3). When FC0 and FC1 are both high, CD mode is selected.

CS8412 (Digital audio receiver)



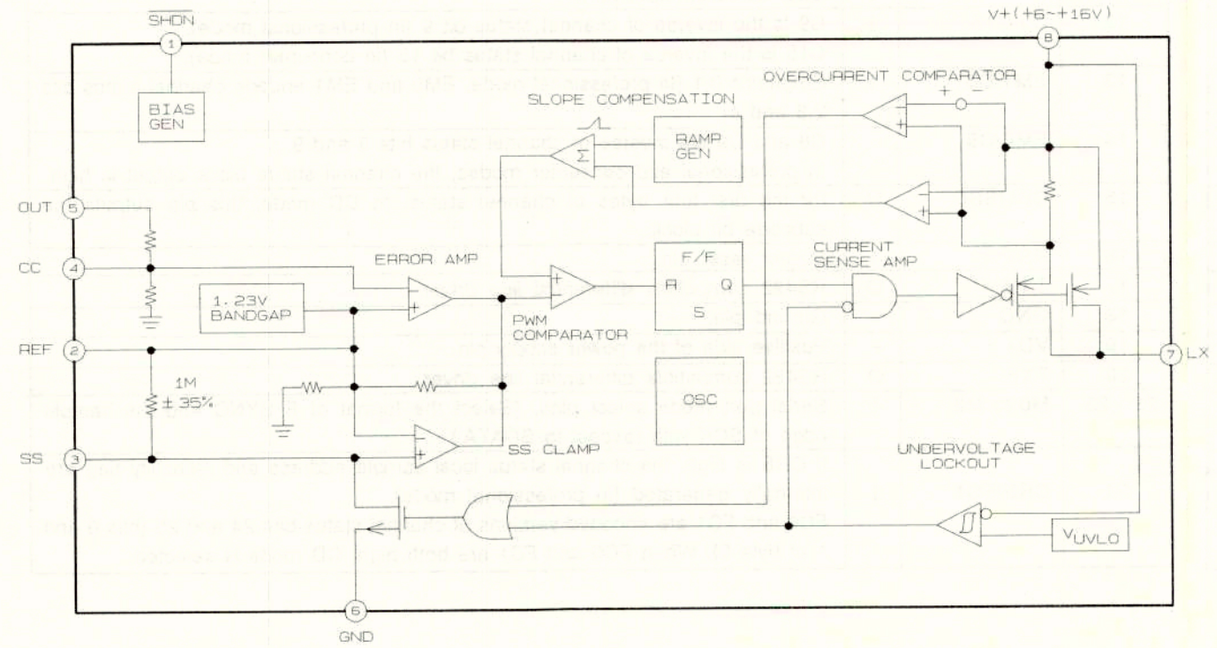
(CONSUMER MODE, CD SUBMODE)

PIN No.	PORT NAME	I/O	FUNCTION
1	$\overline{C7}/\overline{C3}$	I	C7 is the inverse of channel status bit 7 (in professional mode). C3 is the inverse of channel status bit 3 (in consumer mode).
2	$\overline{PRO}$	I	Select the professional mode (low) and consumer mode (high). C1 is the inverse of channel status bit 1 (in professional mode).
3	$\overline{C1}$/FC0	I	FC0 and FC1 are encoded versions of channel status bits 24 and 25 (bits 0 and 1 of byte 3). When FC0 and FC1 are both high, CD mode is selected.
4	$\overline{C6}/\overline{C2}$	I	C6 is the inverse of channel status bit 6 (in professional mode). C2 is the inverse of channel status bit 2 (in consumer mode).
5	MCK	I	Master clock input pin.
6	SCK	I	Serial clock input pin.
7	FSYNC	I	Frame sync input pin.
8	SDATA	I	Audio data serial input pin.
9	V	I	Validity bit serial input port.
10	C/SBF	I	C is the channel status serial input port (in professional & consumer modes). This pin inputs the CD subcode frame clock (CD mode).
11	U	I	User bit serial input port.
12	$\overline{C9}/\overline{C15}$	I	C9 is the inverse of channel status bit 9 (in professional mode). C15 is the inverse of channel status bit 15 (in consumer mode).
13	EM1/$\overline{C8}$	I	Emphasis 0,1 (In professional mode, EM0 and EM1 encode channel status bits 2,3 and 4).
14	EM0/$\overline{C9}$		C8 and C9 are inverse of channel status bits 8 and 9. In professional and consumer modes, the channel status block output is high
15	CBL/$\overline{SBC}$	O	for the first four bytes of channel status. In CD mode, this pin outputs the subcode bit clock.
16	$\overline{RST}$	I	Master reset pin.
17	TXN	O	RS422 compatible differential line driver.
18	GND	–	Ground pin.
19	VD+	–	Positive side of the power supply pin.
20	TXP	O	RS422 compatible differential line driver.
21 - 23	M0 to M2	I	Serial port mode select pins. (Select the format of F SYNC and the sample edge of SCK with respect to SDATA.)
24	CRE/FC1	I	If CRE is high, the channel status local sample address and reliability flag are internally generated (in professional mode). FC0 and FC1 are encoded versions of channel status bits 24 and 25 (bits 0 and 1 of byte 3). When FC0 and FC1 are both high, CD mode is selected.

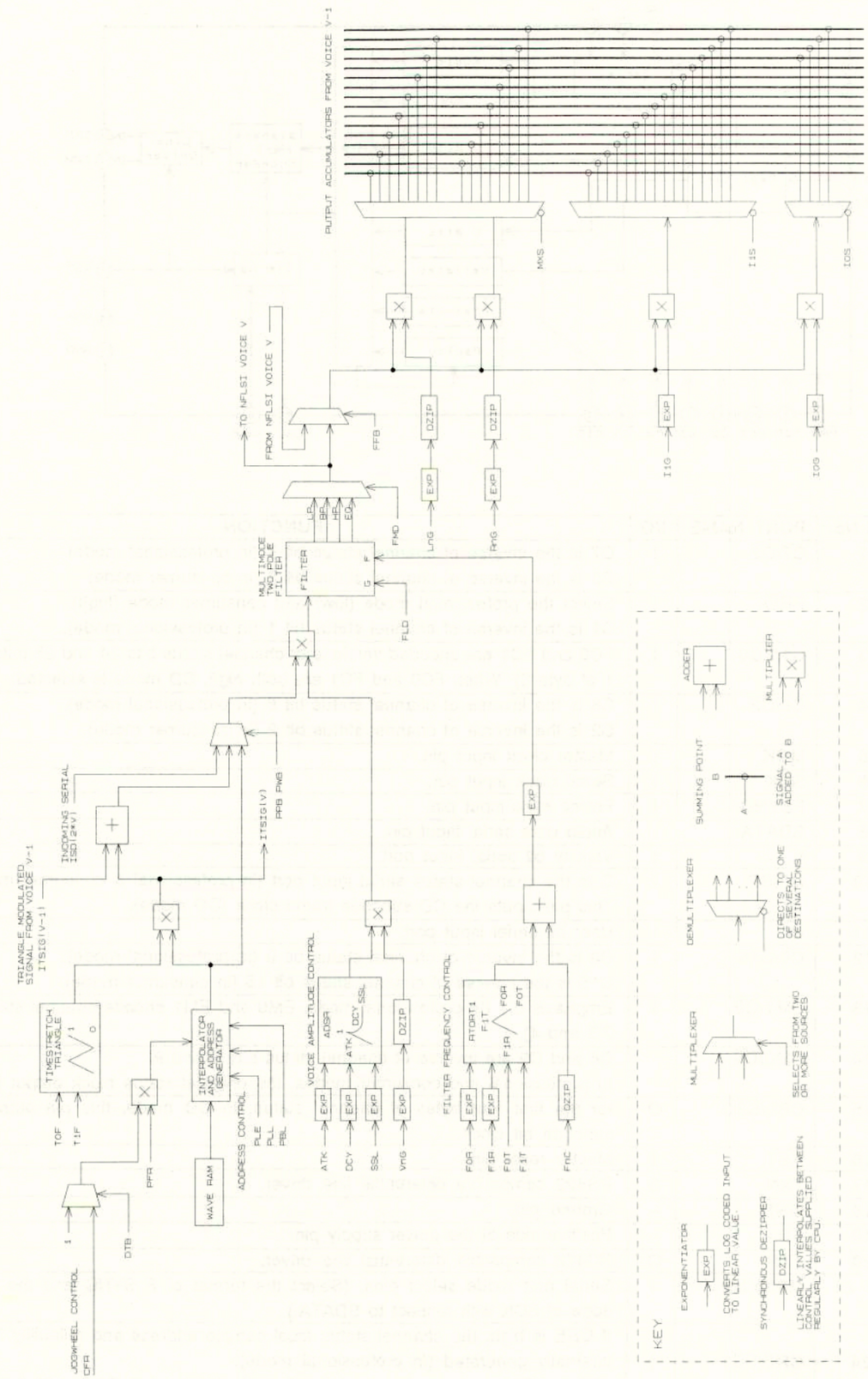
CXD1185AQ (SCSI controller)

PIN No.	PORT NAME	I/O	FUNCTION
1 to 4	A3 - A0	I	Registor selecter, 0 to 3 bit
5, 7 to 10, 12 to 14	$\overline{DB0}$ - $\overline{DB7}$	I/O	Data bus on SCSI bus
15	$\overline{DBP}$	I/O	Data bus on SCSI bus, Odd parity
17	$\overline{ATN}$	I/O	ATN signal on SCSI bus
18	$\overline{BSY}$	I/O	BSY signal on SCSI bus
19	$\overline{ACK}$	I/O	ACK signal on SCSI bus
20	$\overline{RST}$	I/O	RST signal on SCSI bus
22	$\overline{MSG}$	I/O	MSG signal on SCSI bus
23	$\overline{SEL}$	I/O	SEL signal on SCSI bus
24	$\overline{C/D}$	I/O	C/D signal on SCSI bus
25	$\overline{REQ}$	I/O	REQ signal on SCSI bus
28	$\overline{I/O}$	I/O	I/O signal on SCSI bus
29	$\overline{RES}$	I	Reset all registors, L-active
30	$\overline{CS}$	I	Chip select, L-active
31	$\overline{RE}$	I	Read internal registor, L-active
32	$\overline{WE}$	I	Write internal registor, L-active
33 to 40	XDB7 - XDB0	I/O	CPU bus data
42	IRQ	O	Interrupt request
43	DRQ	O	DMA request
44	$\overline{DACK}$	I	DMA acknowledge, L-active
45	$\overline{WED}$	I	Write strobe for data bus, L-active
46	$\overline{RED}$	I	Read strobe for data bus, L-active
47 to 54	HDB0 - HDB7	I/O	Data bus
55	HDBP	I/O	Data bus, parity
57	CLK	I	Clock input
59	$\overline{INIT}$	O	Select signal when initiator action
60	$\overline{TARG}$	O	Select signal when target action
61	P0	I	ADSENSE signal input
62	P1	O	RXINH signal output
63	P2	I	ADSENSE 2 signal input
64	P3	–	Not used
6, 11, 16, 21, 27, 41, 56	GND	–	Ground
26, 58	VDD	–	+ 5 V power supply

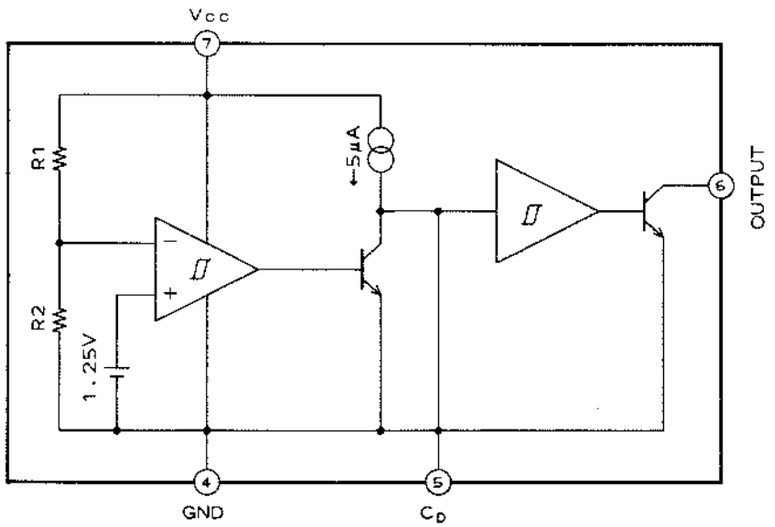
MAX738A (DC-DC converter (12 V to 5 V))



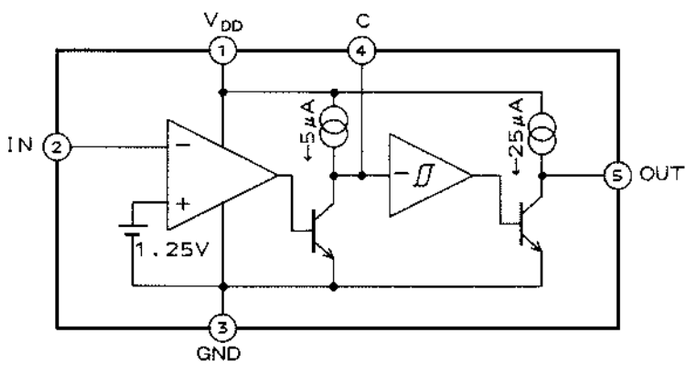
L6044 VM (32 voice DSP)



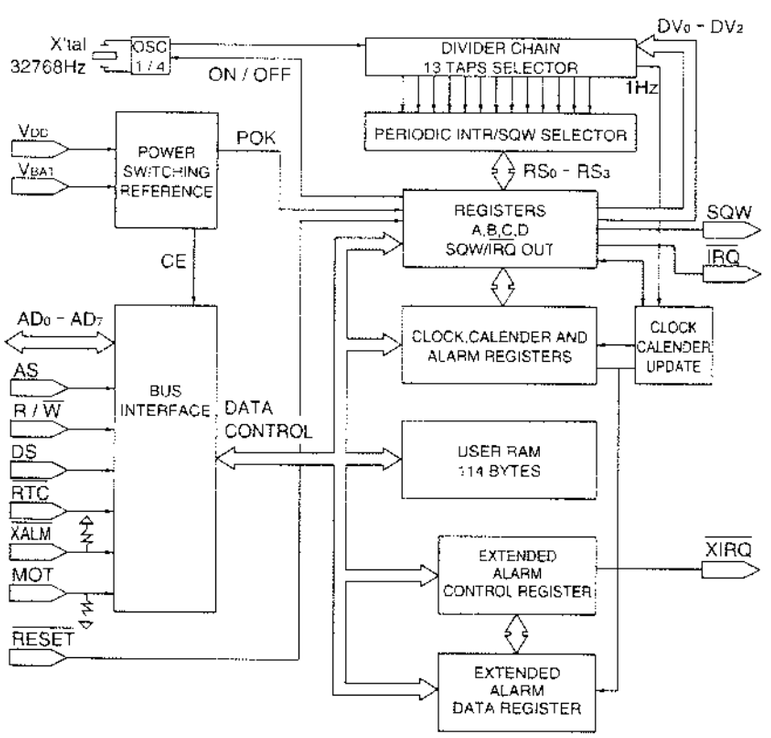
M51953BFP (System reset pulse generator.)



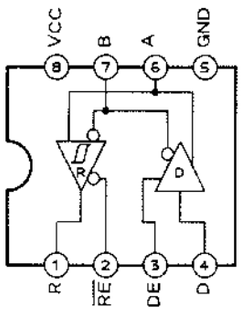
M51957BL (System reset pulse generator)



RTC-6593 (Real time clock /Non-volatile RAM)



SN75LBC176D (Differential bus transceiver)



TRUTH TABLE

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

H= "H" Level , L= "L" Level
X= "H" or "L" Level, Z=High-Impedance

UPD72068GF (Floppy disk drive controller)

PIN No.	PORT NAME	I/O	FUNCTION
1	2SIDE	I	Two Side.
2,9,23,42,43, 65,71	NC	–	No Connection.
3	FLT	–	Fixed at "H"
4	SIDE	O	Side Select.
5,8,55,58, 61,64,68,72	GND2	–	Ground 2
6	FLTR	–	Not used
7	HDLD	–	Not used
10	LCT	O	Low Current.
11	VDD1	–	+5 V.
12	VDD2	–	+5 V.
13	ENPCS	I	Enable Pre-Compensation.
14	ACTL	I	Active Level.
15	$\overline{\text{ENRW}}$	–	Fixed at "L"
16	RSEL	–	Fixed at "L"
17	MSEL	–	Fixed at "L"
18	RESET	I	Reset.
19	$\overline{\text{RD}}$	I	Read.
20	$\overline{\text{WR}}$	I	Write.
21	$\overline{\text{CS}}$	I	Chip Select.
22	A0	I	Address 0.
24,29,33,47,50	GND1	–	Ground 1.
25~28 30~32,34	D0~D7	I/O	Data Bus.
35	DMARQ	–	Not used
36	$\overline{\text{DMAAK}}$	–	Fixed at "H"
37	TC	I	Terminal Count.
38	INT	O	Interrupt Request.
39	FMT	I	Format.
40,41	DR0,DR1	I	Data Rate.
44	INDEX	–	Index.
45	PCS0	–	Fixed at "H"
46	PCS1	–	Fixed at "L"
48,49	XA1,XA2	I/O	Crystal A connecting terminals.
51	XB1	–	Fixed at "H"
52	XB2	–	Not used
54,56	DEN0,DEN1	–	Not used
57,59,60,62	DS0 ~ DS3	O	Data select output.
63,66,67	EM1 ~ 3	–	Not used
69	EMO	I	Enable Motor
70	DIR	O	Direction.
73	STEP	O	Step.
74	WDATA	O	Write data.
76	WE	O	Write Enable.
77	TRK0	I	Track 0.
78	WPRT	I	Write Protected.
79	RDATA	I	Read Data.
80	READY	I	Ready.